CMOS post-processing for monolithic microsystems

Jurriaan Schmitz

MESA+ Institute for Nanotechnology, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands

The semiconductor industry is adjusting focus towards the so-called “More than Moore” innovation. By this is meant that microchip progress may not (or not only) follow from Moore’s Law and its resulting dimensional scaling, but can also come from the addition of new components, new layers and new functions inside the microchip itself. Examples are the introduction of passive RF components, biosensors, and 3D integration.

This new innovation paradigm offers great opportunities for the field of microelectronics. Rather than the unidirectional scaling improvements of CMOS and memory technologies, leading to ever higher performance microprocessors and cheaper memory, diversification will lead to entirely new microsystems. Recent examples are the CMOS active pixel sensor, now embedded as cameras in many handheld consumer products, and human-implantable electronics for medical purposes.

In this work, several recent breakthroughs in this field are discussed, with a focus on technology.

The first microsystem presented, fabricated by CMOS post-processing, is a miniaturized gaseous radiation detector working along the principle of a Multiwire Proportional Chamber [1]. It consists of a CMOS microchip with an array of 256x256 bondpads at its surface, the so-called Timepix chip. Each bondpad is connected to a fast charge-sensitive preamplifier. On top, insulating pillars and an aluminum grid are fabricated, using spin-coating of SU-8 and sputtering. The resulting detector allows fast 3D radiation imaging with high position resolution.

The second CMOS-integrated device is a thin-film solar cell [2]. Envisaged as the ultimate means to power an autonomous sensor node (“Smart Dust”), a thin-film solar cell offers high power levels (even indoor) using very little material, with excellent long-term reliability. Experiments have shown that both a-Si and CIGS solar cell technology are compatible with CMOS. Key was to employ existing technologies, as thin-film solar cells are already optimized for low thermal budget and low stress.

The third device presented is a MEMS resonator fabricated at CMOS backend compatible temperatures using germanium-silicon technology [3]. By careful tuning of the polycrystalline germanium-silicon deposition process, low-stress layers with very low resistivity were obtained using in-situ boron doping. By patterning a very narrow gap in the capacitively transduced device, very high quality factors and relatively low motional impedances were recorded.

Finally, we will share recent results on novel materials for CMOS post-processing, in particular related to the integration of optical functionality on a CMOS chip.