Investigation on Impact of Different Defects based on Different Trap Energy Level in the Framework of Two-Stage NBTI model

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Charges in gate dielectric significantly degraded the p-MOSFET device performances particularly due to NBTI phenomenon. The validation of NBTI effects on device and circuit performance require accurate model to ensure reliable prediction during design phase. Previous works in simulation-based study in assessing the degradation level of p-MOSFET devices [1–4] and circuits [5, 6] specifically on NBTI reliability issues rely on R-D model. However, the R-D model neglect the existence of hole trapping effect in pre-existing bulk oxide traps and switching oxide trap which found under fast pulse measurement method [7, 8]. To account for the contribution of hole trapping effect, a simulation study based on two-stage model is developed [9–11]. The simulation based study utilized this model had been conducted by [12] based on trap energy level defined in [11], [13]. However, experimental work found that each defects are distributed below the valence band edge, within energy band gap and above conduction band edge for the as-grown hole traps, created defects and antineutralization positive charges respectively [14]. The accurate model which correctly includes the contribution of defect precursor, switching oxide trap and interface trap which distributed below, within and beyond band gap respectively has not been established yet. Within the framework of two-stage NBTI model, we re-defined the defects’ energy levels similar to as experimentally observed whereby the precursor, S1 is the as-grown hole traps, switching oxide, S2 is the created defects while antineutralization positive charges is the interface trap, S4. In this paper, we investigate and validated the density of states for each trap specifically defined below, within and beyond energy band gap using Sentaurus TCAD simulator. The simulation accuracy of new energy level for each traps are validated based on the density of states for each trap subsequent to a wide stress bias under room and high temperature which the results are explained with regard to the characteristics for each as observed in experiment. The correlation of defects contribution in the degradation as shown in Fig. 1 (a) is assessed based on the time exponent, n. For Vgstress higher than -1.5 V at 398.15K, the n ~ 0.2 which has been observed in [15]. Contribution from S1 is the lowest at higher stress voltage. During this stress level condition, the S2 is more than S4. However, S2 is saturate as the stress voltage increased while the S4 do not saturate which also exhibit in the experimental work [14]. The S4 is also thermally accelerated which in agreement in [14] as higher stress temperature exhibits 71% increased as compared to during room temperature. Fig. 1 (b) shows that the default energy level exhibits maximum of n ~ 0.1 during higher Vgstress which imply that the degradation is disturbed by the pre-existing defect signal [7, 8]. Hence, prediction using default energy level include both contribution from pre-existing defects, S1 as well as generated defects (S2 and S4) lead to invalid lifetime prediction as discussed in [15].

Fig.1 (a) New defined energy level (b) default energy level


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