Nanometer ASIC Seminar

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This comprehensive seminar explains, in depth, all of the numerous steps involved in developing an ASIC, at nanometer feature sizes (like 32-nm and below).

The IC development process has become so complex that few professionals are fully conversant with all phases in the flow—especially with the feature size approaching the scale of a few dozen *atomic layers*. By drawing on a broad range of experience at such Silicon Valley companies as Intel and Synopsys, and a university background in solid-state physics, the speaker explains key concepts at an intuitive level.

Partitioning the ASIC development flow into the six broad phases in Fig. 1, the seminar covers hands-on *design*, including RTL coding in SystemVerilog, IP-based design, and on-chip RF/mixed-signal design.

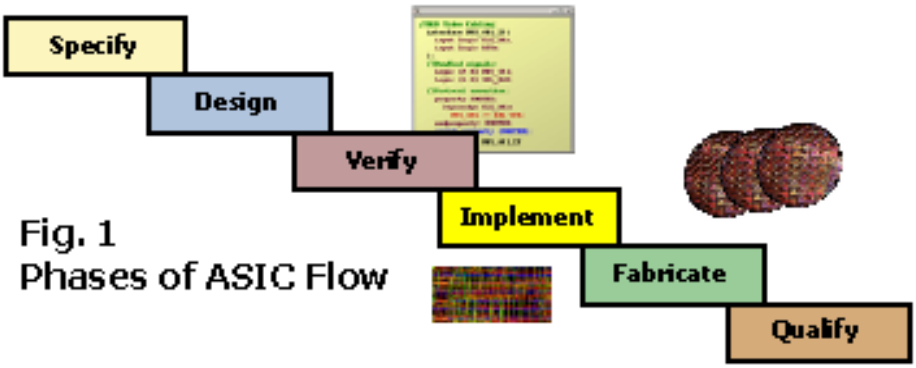

Fig. 1
Phases of ASIC Flow

In the next phase, the thousands of lines of RTL code must be *verified* against the original specifications. Logic simulators, the traditional workhorse tool, have run out of steam as run times can exceed whole days.

|Functional equivalence checkers are a supplementary tool that involves no advancement of time. Another supplemental verification tool is the **assertion** [1]—a feature of the SystemVerilog language that offers *localized* debug statements that can directly check out detailed design or system functions from the specs.

The next phase *implements* the fully-verified design database, using logic synthesis and physical design.

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Relying on his experience at Synopsys, the speaker includes many insights into how such EDA tools as ***Design Compiler*** and ***IC Compiler*** really work. The concept of the *standard cell,* which these tools rely on, is explained in depth: including logic function, propagation delay, silicon area, power consumption.

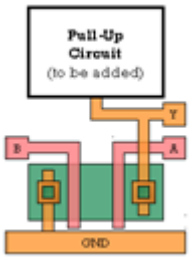

Fig. 2 Typical CMOS NAND2 Standard Cell

Once the ASIC is floorplanned and placed and routed, timing closure is met, and design-rule violations are resolved, the development flow reaches a milestone: *tape-out.* Little-understood concepts, like taping out the chip's huge GDSII database, are demystified.

In the next phase, the venue shifts from design house to silicon foundry. Based on his early years in one of Intel's first wafer fabs, the speaker explains how GDSII data is imprinted, layer by layer, onto silicon.

The last phase includes packaging (flip-chip and 3-D) and testing, validation, shmoo plots, process corners, and other steps to *qualify* the new IC for production.

An appendix offers a tutorial on finFET transistors—the biggest departure from planar MOS since Gordon Moore first began to plot his now-famous law.

[1] C. Dancak, *Preponed Timing in RTL Assertions: A Tutorial Example,* 2016