HDL Application for Digital Synthesis in FPGA

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HDLs, like VHDL, Verilog and System Verilog are widely used for digital design. Actually HDL is a common tool, when you are going to implement something in FPGAs or CPLDs. HDLs make the process very flexible and allow user to implement very different algorithms and structures without deep investigation of the architecture the chip used.

However, professional designer is typically interested in creating design with superior performance, meeting various requirements. It requires some more specific knowledge and experience, than just a good level of understanding HDL. Moreover, HDL often produces a confusing results, if use it without clear understanding of what you are going to obtain. This paper is focused on some details of FPGA-based digital synthesis using VHDL in Vivado environment as an example.

One of the most important issues, which is necessary to remember, is that Vivado is focused on the synthesis of a digital device, built on Configurable Logic Blocks (CLBs), present in the FPGA, selected for the implementation. It unlikely is able to create something, which cannot be directly built using CLBs.

Second issue is that Vivado has some settings, intended to meet various criteria imposed by user, but these settings are just recommendations. You can recommend to use this or that technique, however, if the compiler finds a solution, which seems “better”, it will use its solution.

Third issue is that FPGAs have some specific modules, like Look-Up-Tables (LUTs), which make classic approaches to logical synthesis useless. Using LUTs implies, that logical functions are implemented as memory tables rather than a sequence of gates.

All these issues, mentioned above, make the process of design rather specific, based on abstract considerations and understanding how the compiler creates final circuitry. There are several important areas, where one should be careful, using HDL’s opportunities. Using variables may result in unpredictable circuitry, however synthesizable and workable. Improper use of sequential operations can create situations, when some signals or operations are excluded from synthesis. Some descriptions can be compiled using multiple driven signals, which are synthesizable, but obviously not workable. However in such cases various warnings are generated, and a user can recognize the result on an early stage.

Synthesis of fast circuits has some specific features, requiring much attention to critical paths and timing rules. In this case user can want to force Vivado to create circuitry, which looks unexpected. This process also requires some specific skill. Metastability is an important issue, when you need to provide really high reliability, for example, high value of MTBF. It requires specific circuitry as well. In fact most part of solutions is more or less well-known and can be implemented using IP cores or coding templates, provided by Vivado or third part.

Professional designer should combine good knowledge of HDL, synthesis tool, digital devices and use all these issues with careful attention to obtain good results.

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