

Interconnect Challenges of ULSI Devices Beyond 10 nm

Technology Nodes

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ULSI technology includes front-end-of-line (FEOL), which is the first portion of Integrated circuits (IC) fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor. The back-end-of-line (BEOL) is the second portion of IC fabrication where the individual devices get interconnected with wiring on the wafer. Modern ICs are very compact, incorporating up to several billions transistors and other electronic components in an area of about 1 cm². All transistors and other IC components must be electrically interconnected to provide the proper functionality. The width of the conducting lines and space between them is becoming smaller and smaller as the technology advances; now they are of the order of a tens of nm.

With the aggressive scaling of advanced integrated circuits to nanometers levels, signal delay caused by the interconnects became increasingly significant compared to the delay caused by the gate. In addition, the cross talk noise and power dissipation became much more important in circuit performance. To reduce the resistance- capacitance (RC) delay, the industry has replaced the Al conductor by Cu (lowering resistance) and Silicon Dioxide (SiO₂) by materials with a lower dielectric constant, low-k (lowering capacitance). In order to reduce the dielectric constant of a material, either atomic groups with a small polarizability can be inserted or the electronic density can be lowered. The density has a stronger effect on the k-value than the polarizability, since the density can be lowered till zero (air-gaps), achieving unity as k-value. The ultra low-k materials introduction in Cu technology has been much slower than anticipated in the ITRS Roadmap. The introduction of porosity in low-k materials has increased the level of complexity tremendously. In this presentation, the challenges appearing during the integration of ultra low-k dielectrics will be discussed, since a proper understanding of these issues is essential for downscaling of the interconnect system. The extreme vulnerability of porous low-k to processing - induced damage (accompanied with the loss of dielectric performance and reliability) demands a continuous innovation of materials, processes and integration approaches. Recently developed new materials and innovation solutions for low-k integration will also be discussed.