NanoCMOS and Tunnel FETs for the end of the Roadmap

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Introduction: Challenges

We are facing **dramatic challenges** dealing with future nano-scale devices:

- *Performance*
- *Power consumption* ↑
- **Many new materials** and **device architectures** needed (transistors, memories)
- Device integration (2D, 3D)
- **Interconnects** (Traditional, Optical, RF, carbon/2D materials)
- Ultimate technological processes (EUV, immersion multiple patterning, multi ebeam, imprint lithography, self-assembly)
- **Novel functionalities** (sensing, EH, RF) using **nanodevices** and **nanomaterials**

=> needing **disruptive approaches especially new devices using innovative materials**
Big challenges to continue More’s law:

**Node-to-Node Transistor scaling:**
- 50% area reduction
- 25% performance increase @ scaled $V_{DD}$
- 20% power reduction
- 30% cost reduction
  - every 2-3 years

⇒ Novel Lithography, Materials, Architectures, Physics, State variables…
  using **green & sustainable technologies** / power_scarce & toxic materials

⇒ Several $10^9$ devices/circuit in Electronics: complex
⇒ Human kind: $100 \times 10^{12}$ Synapses/Bacteria in brain/gut: **extremely complex** (sustainability / link with toxicity)! **Very far from this performance/low power!**
Slowdown of Vdd scaling and increase of subthr. Leakage:

$\Rightarrow \uparrow$ of dynamic and static power consumption
Possible Solutions for ULP Systems

- Very big amount of exchanged and stored data
- Exponential $\uparrow$

$\Rightarrow$ Reduction of energy consumption: main challenge for future electronic systems

$\Rightarrow$ A number of innovations will be needed:

- transistor, memory, devices, interconnects technos
- circuit design techniques
- systems architectures
- embedded software
Possible solutions

- **Ex:** Transistors: energy consumption $\sim 10^4 \text{kT}$ today
  $\Rightarrow$ limit $\sim \text{kT}$ (*landauer limit for irreversible switching*)

$\Rightarrow$ could be reached with nanodevices using **new physical concepts/materials/architectures** and technology breakthroughs

$\Rightarrow$ strong ↓ static (*I*leakage) and dynamic (*CV*^2) circuit consumption, with e.g.:

- electron transport (*FD-SOI, MG, Nanowires, CNT, TFET, FeFET*)
- spin (*SpinFET*)
- electromechanical properties (*NEMS*)
- combination with **alternative materials:** Ge, III-V, Fe, 1D, 2D...
Scalability for CMOS: Natural Length

\[ \lambda_n \approx \sqrt{\frac{1}{n \varepsilon_{ox}} \frac{\varepsilon_{sc}}{t_d t_{ox}}} \]

- \implies decrease:  
  - tox
  - td (depletion width/Si film/NW diameter) -> SOI/FinFET/multi-gate/GAA/2D
  - \varepsilon_{sc} (Si better / Perf. boosters Ge and III-V)

- \implies increase:  
  - \varepsilon_{ox} (high k)
  - n (number of gates)
Power challenge due to subthreshold slope limit and lower limit in energy per operation

Reducing threshold voltage by 60mV increases the leakage current (power) by ~10 times

\[ \text{Emin} \sim C \cdot S^2 \]

\[ \text{Vdd}_\text{min} \sim S \]

(Hanson, IEEE TED 2008)

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Possible solutions for reducing Sub. Swing

-Solutions for reducing $S$:

$$S = \frac{\partial V_g}{\partial (\log I_d)} = \frac{\partial V_g}{\partial \psi_S} \frac{\partial \psi_S}{\partial (\log I_D)} = (1 + \frac{C_s}{C_{ins}}) \frac{kT}{q} \ln 10$$

$m$ less than 1

$n$ less than $(kT/q)\ln 10$

$\Rightarrow$ Decrease of the transistor body factor $m$: UTB/MG/NW/CNT/Graphene/2D ($m \sim 1$) or $m < 1$: NC-FET with Fe materials, MEMS/NEMS ...

$\Rightarrow$ Reduction of $n$: modification of the carrier injection mechanisms (or low $T^\circ$): I.I. ($high V$), BTBT with novel materials ...

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Advanced bulk & **FD-SOI** MOSFETs: Scaling (td), Power (S) & Performance (μ)
Subthreshold swing of FD SOI MOSFETs

⇒ Down to 60 mV/dec for UTB at 300K

Impact of ultra-thin BOX on FD SOI DIBL and leakage

Channel thickness necessary to have a DIBL of 100mV/V as a function of channel length.

[F. Andrieu et al., VLSI 2010]
**Multi-gate** for very low power and HP:
Scaling (td, n), Power (S) & Performance (µ)

=⇒ Fully Inverted MOSFET (Balestra EDL’87)
Subthreshold swing in double-gate SOI MOSFETs


Numerical simulation of subthreshold swing for various types of extremely thin ($t_{si} = 10$ nm) SOI MOSFETs ($L_g = 0.05$ $\mu$m)

Single gate
($t_{ox1} = 3$ nm and $t_{ox2} = 0.38$ $\mu$m),

double gate
($t_{ox1} = t_{ox2} = 3$ nm),

various dopings
($N_a = 10^{15}$ cm$^{-3}$ and $N_a = 5 \times 10^{17}$ cm$^{-3}$)

→ Improvement of the swing:
- with reducing the Si film doping
- with a back gate accumulation ($V_{g2} = -40$ V)
- for a double gate SOI MOSFET
  with volume inversion
DIBL versus device architecture: 1G, 2G
Comparison of $S$ for sub-10nm Lg for:

\textbf{Ω-gate sSi} and \textit{InGaAs NW, GAA CNT (≠d), DG sSi UTB}

Very good $S$ down to 5nm Lg, but…. $>60\text{mV/dec}$!

(simul. M. Luisier, IEDM11):
Hybrid Si/TMD Using Solid CVD Few-Layer-MoS2 Stacking

Min-Cheng Chen, IEDM 2014

Si/MoS2/Hf02/TiN Hybrid FinFET and NW

μ ↗ in Si/MoS2 vs Si FinFET (but need to be evaluated at given Ioff)

Id ↗ in FinFET & NW for Si/MoS2
MoS2 with 1G SOI and DG with 1-3 layers vs Si UTB DG MOSFETs (simul.)

W. Cao, IDEM 2014

Best S and DIBL for DG MoS2 (1L)
But similar as sSi $\Omega$-gate NW with d=3nm
Also need good Nit control
Comparison of scaling limit for TMDs, Phosphorene/BP and Si
(Modeling, P. Zhao - IEDM’15)

Lgmin vs Tchannel for 2G Si ($\epsilon=12$), BP ($\epsilon=9$, Tch=0.3N), TMDs ($\epsilon=4$, Tch=0.7N)

=> Best for TMDs / BP

(N=nb of layers, $\epsilon_{ox}=4$)

(Rem: high effective mass along the channel for 2D materials => S-D tunneling could ↓ / Si for sub-5nm Lg)
Mobility vs bandgap for various 2D materials and UTB semiconductors

(G. Fiori - IEDM’15)

\[ \mu \uparrow \text{ when bandgap } \downarrow \]

BP good trade-off but many technological issues
Ab-initio simulation of 2D MOSFETs

Best Idon for Black Phosphorous (AC: transport parallel to the armchair configuration) for n and p devices compared to several TMD channels (no Rsd)

M. Lusier, IEDM 16
Bandgap engineering in 2D materials by Electric field: Graphene

(Experimental, T. Chu - IEDM’15)

Ion/Ioff and Bandgap ↗ in Bilayer Graphene Ribbon (100nm) with transverse Electric Field (front 7nm HfO2 and back gate)
Bandgap engineering in 2D materials by Electric field: TMDs
(Experimental, T. Chu - IEDM’15)

Bandgap and Ion/Ioff↓ when Vgb ↑ for Bilayer MoS2 inducing a Semi-Metallic state
Bangap in 1D structures

![Graph showing bandgap energy vs. nanowire diameter for different materials]

Ansari, Nano Letters 2012

Bangap ↑ when NW diameter ↓ for Semiconductors and Semimetals

=> Semimetal -> Semiconductor
Example: Sn NW (Ab-initio simulations)

⇒ No doping in channel and S/D
⇒ Very good result but very small d needed <2nm for same Eg as Si (similar as graphene nanoribbon)
⇒ Need very good d control (variability)

Ansari, Nano Letters 2012
Solutions for reduction of $S$ below 60mV/dec

- Strong reduction in Vdd and Emin possible using new physics/materials/devices with sub-60mV/dec subthreshold swing (limit of MOSFETs at RT):

  $\Rightarrow$ **Energy filtering**: *Tunnel FET* (MOS-NW-CNT- or Graphene-based): BtB tunneling to filter energy distribution of electrons in the source (cuts off the high energy $e$/Boltzmann tail resp. for 60mV/dec): $PB \Rightarrow Ion$

  $\Rightarrow$ **Internal voltage Step-up**: *Ferroelectric gate FET* (inducing a negative capacitance to amplify the change in channel potential induced by the gate): $PB \Rightarrow long$ switching times

  $\Rightarrow$ **NEMS/NEMFET/relay**: $PB \Rightarrow$ voltage scaling, reliability

  $\Rightarrow$ **Hybrid devices**: Fe TFETs, Phase Change materials, Atom Scale filament...
The quasi-ideal switch

- **Quasi-ideal binary switch:****
  - 2 stable states (off, on)
  - $I_{on}$: as high as possible
  - $I_{off}$: as low as possible
  - abrupt swing (mV/decade)
  - very fast (<ns)

MOSFET Switch: 
SS~60mV/dec @ RT

Small Swing Switch
Small swing switch best parameters

To outperform CMOS:

- $I_{on}$: range of hundreds of $\mu$A
- $S_{avg}$ far below 60mV/dec for at least 4-5 decades of $I_d$
- $I_{on}/I_{off} > 10^5$
- $V_{dd} < 0.5V$
Reduction of $S$ below 60mV/dec:
Very promising $\Rightarrow$ TFETs

- Very promising ones, TFETs, use gate-controlled pin structures with carriers tunneling through the barrier and not flowing over:

$\Rightarrow$ Interband tunnelling in heavily-doped $p+n+$ junction with a control of band bending with $V_g$ and a reversed bias $p-i-n$

$\Rightarrow$ Ambipolar effect has to be suppressed by asymmetry in the doping level or profile, or the use of heterostructures
Tunnel FET

**OFF-state**
- $V_d = $ positive
- $V_g = 0$
- *no current flows*

**ON-state**
- $V_d = $ positive
- $V_g = $ positive
- *barrier thin, current flows*

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Tunnel FET

- **Opportunities**: reduce by decades standby power
- **Challenges** for Tunnel FETs:
  - bandgap engineering
  - *on-state* performance improvement needed
  - exploitation of innovative (nano)structures

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Major parameter for BTBT: Transmission probability

\[
I_{BTB} \propto T_{WKB} \approx \exp\left(\frac{-4\lambda\sqrt{2m^*E_g^{1.5}}}{3\eta(\Delta\Phi + E_g)}\right)
\]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Means of improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>(m^*)</td>
<td>Small effective tunnel mass, SiGe, III-V, CNT</td>
</tr>
<tr>
<td>(E_g)</td>
<td>Source in SiGe, III-V heterostructures, strain CNT</td>
</tr>
<tr>
<td>(\lambda)</td>
<td>3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric</td>
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Tunnel FET on Si, SGOI, GOI

$S=42\text{mV/Dec}$, $I_{\text{off}}<0.1\text{pA}$, but $I_{\text{on}}<0.1\mu\text{A}$ at $V_d=1\text{V}$ (exp.)

(F. Mayer et al, IEDM 2008)
III-V channel TFETs

- *InAs TFETs (SG, DG, GAA NW):* small bandgap and electron-hole effective masses inducing BTBT ($V_g=V_d=0.2V$) (M. Luisier EDL 2009, Simul.) :
InAs NW TFETs

F. Conzatti
IEDM 2011
(3D quantum transport simulation)

Subthreshold swing vs gate length for GAA InAs Nanowire TFETs for various wire diameters obtained by quantum simulation.
Comparison of all III-V TFET architectures

⇒ QW-TFET best performance (InAs-GaSb-InAs Quantum Well)

- Graded source H-TFET with $T_{\text{grad}}=5$nm
- Quantum well TFET with $T_{\text{well}}=3$nm
  $Dw=5$nm, $Lg=17$nm, $I_{\text{on}}$ at $I_{\text{off}}=5nA/\mu m$
2D/WTe2 TFET

(Ab-initio quantum simulation, X.-W. Jiang - IEDM’15)

Best results for TMD layers obtained with \textbf{WTe2 TFET} for HP and LOP applications

$V_d=0.5V$, S/D doping $10^{13}$cm$^{-2}$

Performance for $L_g=7$nm close to ITRS HP 2024 requirement

$I_{off}$ degradation for $L_g<5$nm
Comparison of Homojunction and heterojunction 2D TFET
(NEGF quantum simulation, W. Cao - IEDM’15)

Best results for Heterojunction WTe2-MoS2 TFET
2D (MoS2-WTe2) TFET
(Quantum simulation, J. Cao- IEDM’15)

Intrinsic switching energy vs Switching time for various devices: CMOS, TFET (InAs and InAs/GaSb) and 2D TFET MoS2-WTe2 (best results)

Front and back SiO2, 0.35nm gap with $\epsilon=1$, chemically doped MoS2 ($4.10^{12}$cm$^{-2}$) and electrostatically doped WTe2 with $V_{bg}$
Comparison TFET experimental results (<2016)


⇒ $S < 60 \text{ mV/dec for } I_d < 10 \text{ nA/µm}$
- $I_{60}$ is 0.056 $\mu$A/$\mu$m and 0.31 $\mu$A/$\mu$m at VDS = 0.1 and 0.3 V (record exp.)
- Smin~50mV/dec at 300K
- Best Ion for Vg<0.25V (d=20nm, Lg~100nm)

E. Memisevic, IEDM 16
Hybrid device: TFET-FeFET

(a) Transfer characteristic (b) Output characteristic of NC-HTFET. The subthreshold swing is improved significantly with NC. The current of NC-HTFET shows the enhancement with larger $V_{GS}$. Note that both HTFET and NC-HTFET are the same devices for comparison.

Transconductance ($g_m$) vs. $V_{GS}$. The peak $g_m$ is enhanced 118% by the NC integration.

M.H. Lee, IEDM’2013
Hybrid device: Fe FinFET

(K.-S. Li - IEDM’15)

SS ↓ for Fe FinFET / FinFET

Fe material: Hf$_{0.42}$Zr$_{0.58}$O$_2$
Hybrid device: 3D simulation of NC FinFET / FinFET

S ↓ when Lg ↓ for NC-FinFET with Internal Metal Gate due to reduced DIBL

H. Ota, IEDM 16
Hybrid device: Phase-Change Tunnel FET

\[ S \approx 4 \text{mV/dec} \] for the PC-TFET at 300K for 3 decades of Id with vanadium dioxide exhibiting a metal-insulator transition by electrical excitation

E.A. Casu, IEDM 16
Hybrid device: Atom-Scale metal filament MOSFET

- Metal filament (Ag, Cu) formed in Si at the Drain with a sufficient $V$; breakdown of the filament when $V \downarrow$
- $S \sim 5 \text{mV/dec}$ for AS-TFET at $V_d=0.25 \text{V}$ and $300 \text{K}$ for several decades of $I_d$

S. Lim, IEDM 16
Conclusion

• We are facing many challenges, scaling, performance and power reduction which is one of the most important challenge for future nanoscale devices
  => requires new physics and device structures using many novel materials
  => will enable to continue scaling and performance/power improvement

• FD SOI, MG Devices

• F.Inv. MG Nanowires or UTB-2D (with Si, sSi, alternative channel / Ge, III-V, 2D/TMD, BP, HTJ…):

  => Best SCE, S, Ioff, Vdd, P, Emin for MOS-based architectures => Low power/high speed

• TFETs (MG, SOI, GOI, III-V, NW, Strain, HTJ, Grad, QW, 2D), Hybrid FETs:

  => Best Small Slope Switch up to now
  => BTBT, Fe, PC and AS materials or combination allows for sub-60mV/dec S (simulation + experimental results)

  => TFETs simulations show promise for very good S, substantial Vdd reduction and high Ion but technology boosters especially using new materials and devices and additional process improvements are needed to improve real device performance

  => Applications: very low power/low-medium speed, Analog/RF, Sensors…
Thank you for your attention!

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