NanoCMOS and Tunnel FETs for the end of the Roadmap

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Introduction: Challenges

We are facing **dramatic challenges** dealing with future nano-scale devices:

- *Performance*
- *Power consumption* ↑
- **Many new materials** and **device architectures** needed (transistors, memories)
- Device integration (2D, 3D)
- **Interconnects** (Traditional, Optical, RF, carbon/2D materials)
- Ultimate technological processes (EUV, immersion multiple patterning, multi ebeam, imprint lithography, self-assembly)
- **Novel functionalities** (sensing, EH, RF) using **nanodevices** and **nanomaterials**

=> needing **disruptive approaches especially new devices using innovative materials**

IMEP-LAHC

Big challenges to continue More's law:

Node-to-Node Transistor scaling:

- 50% area reduction
- 25% performance increase @ scaled V_{DD}
- 20% power reduction
- 30% cost reduction
  - every 2-3 years

⇒ Novel Lithography, Materials, Architectures, Physics, State variables… using **green & sustainable technologies** / power_scarce & toxic materials

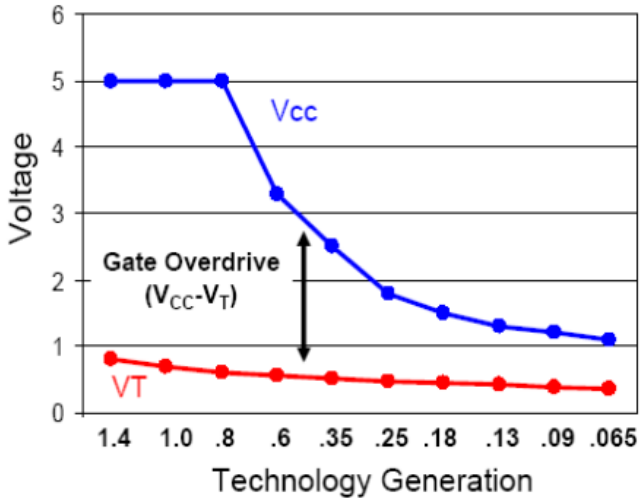
⇒ Several 10^9 devices/circuit in Electronics: complex

⇒ Human kind: 100×10^{12} Synapses/Bacteria in brain/gut: **extremely complex (**sustainability **/** link with toxicity**)**! **Very far from this performance/low power!**

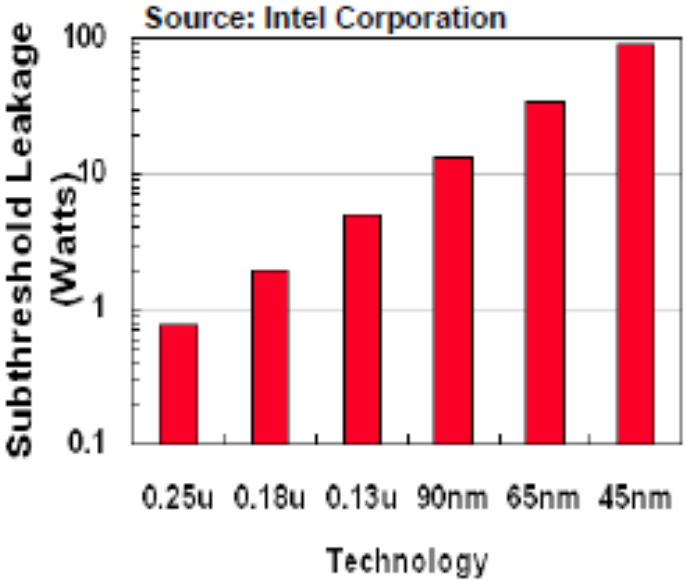
IMEP-LAHC

Slowdown of Vdd scaling and increase of subthr. Leakage:

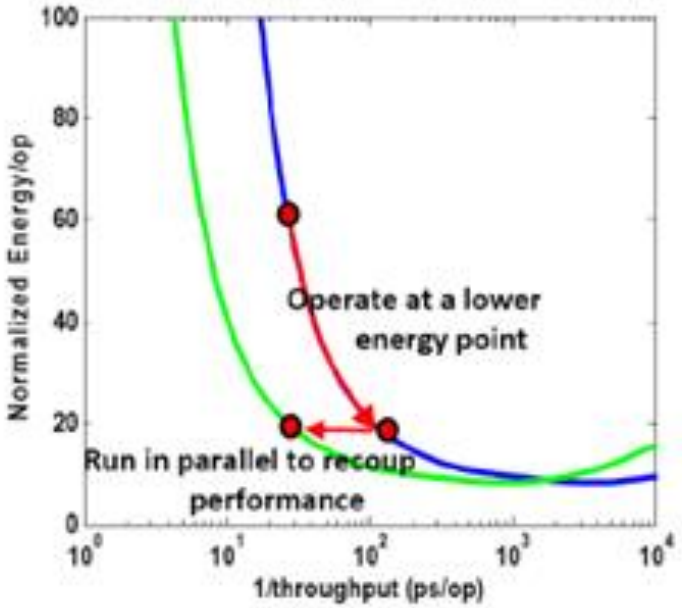
=> ↑ *of dynamic and static power consumption*



(P. Packan (Intel), 2007 IEDM Short Course)



Parallelism (multi-core) is a key technique to improve system performance under a power budget



IMEP-LAHC

Possible Solutions for ULP Systems

- Very big amount of exchanged and stored data
- Exponential ↑

  => Reduction of energy consumption : **main challenge for future electronic systems**

  => A number of innovations will be needed:

  -**transistor, memory, devices, interconnects technos**
  -**circuit design techniques**
  -**systems architectures**
  -**embedded software**

Possible solutions

- **Ex : Transistors :** energy consumption ~ 10^4 kT today
  => limit ~ kT (*landauer limit for irreversible switching*)

  => could be reached with nanodevices using **new physical concepts/materials/architectures and technology breakthroughs**

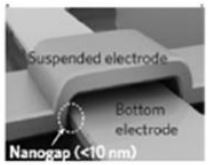
  => strong ↓ static (Ileakage) and dynamic (CV^2) circuit consumption, with e.g.:

  -electron transport **(*FD-SOI, MG, Nanowires, CNT, TFET, FeFET*…)**
  -spin (*SpinFET*…)
  -electromechanical properties **(*NEMS*…)**
  -combination with **alternative materials: *Ge, III-V, Fe, 1D, 2D*...**

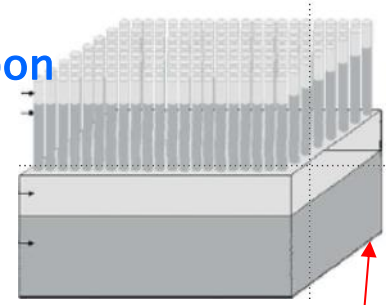
Nanoscale FET roadmap for low energy, scaling, high perf., new functionalities

… IC evolution …

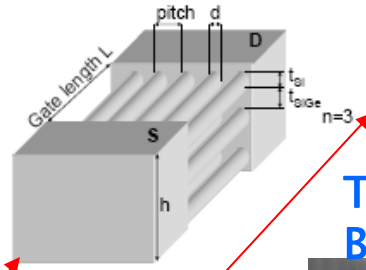
NEMS



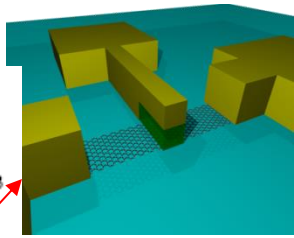
NW/Carbon -based MtM



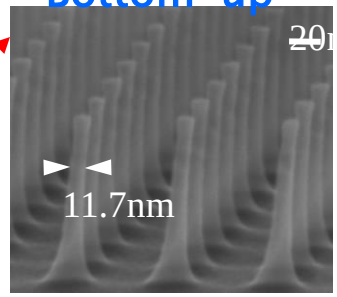
3D-NW



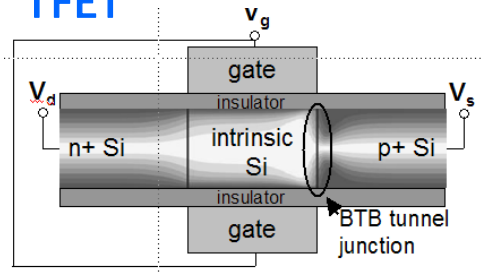
2D-FET

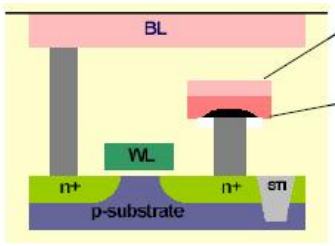


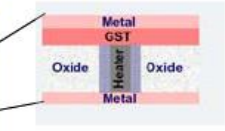
Top-down/ Bottom-up

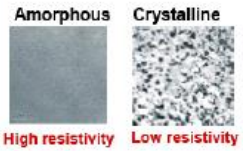


TFET





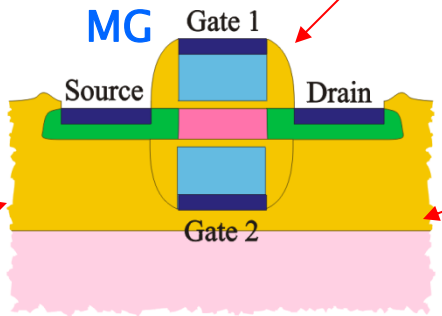


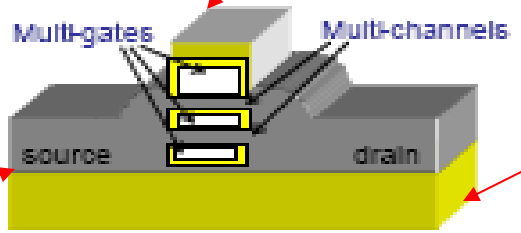


Non-charge/ PCRAM

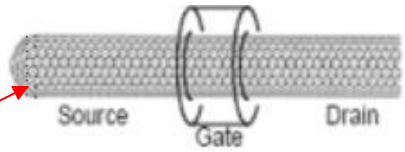
NW/NVM

MG



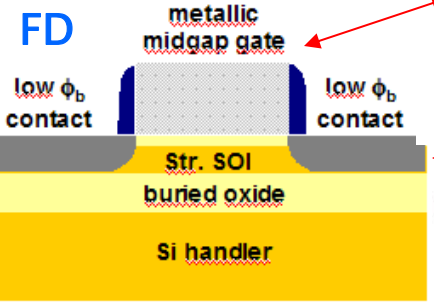


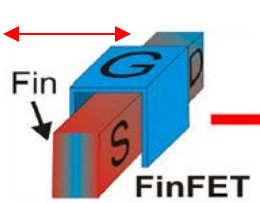
MC

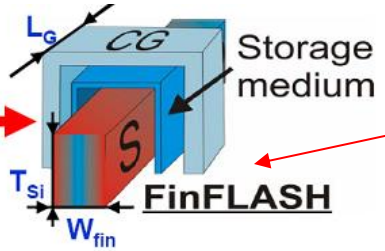


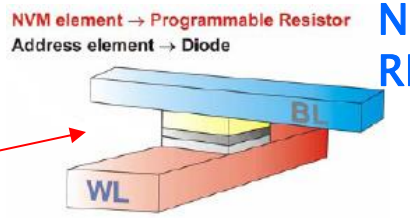
CNT

FD









Non-charge/ RRAM

… IC evolution …

Scalability for CMOS: Natural Length

$$\lambda_n \cong \sqrt{\frac{1}{n}\frac{\varepsilon_{sc}}{\varepsilon_{ox}} t_d \; t_{ox}}$$

⇒ **decrease:** -**tox**

-**td** (depletion **width/Si film/NW** diameter) -> SOI/FinFET/multi-gate/GAA/2D

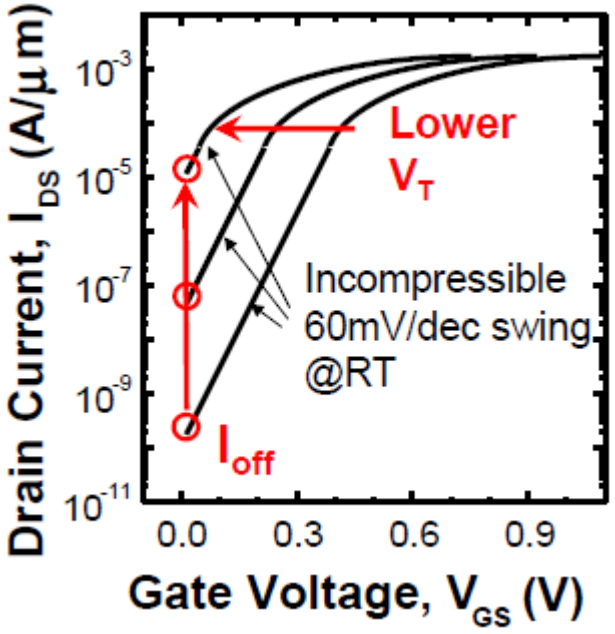
-**Ɛsc** (Si better / **Perf. boosters Ge and III-V**)

⇒ **increase:** -**Ɛox** (**high k**)

-**n** (number of gates)

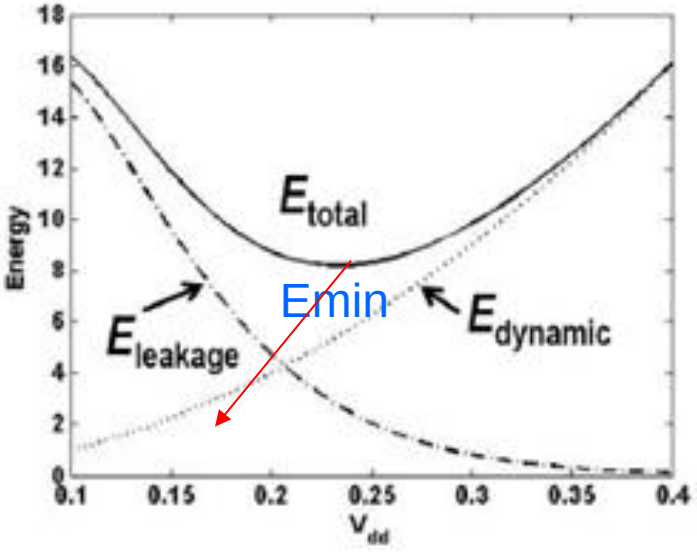
IMEP-LAHC

Power challenge due to subthreshold slope limit and lower limit in energy per operation



Reducing threshold voltage **by 60mV** increases the leakage current (power) **by ~10 times**

CMOS has a fundamental lower limit in energy per operation due to subthreshold leakage



Emin ~ C . S^2
Vddmin ~ S
(Hanson, IEEE TED 2008)

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Possible solutions for reducing Sub. Swing

-Solutions for reducing S:

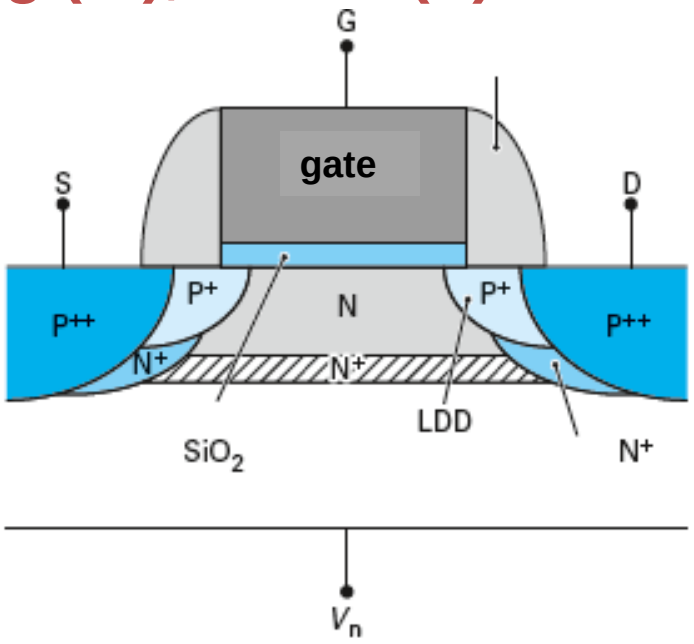
$$S = \frac{\partial V_g}{\partial(\log I_d)} = \underbrace{\frac{\partial V_g}{\partial \psi_S}}_{m} \underbrace{\frac{\partial \psi_S}{\partial(\log I_D)}}_{n} = (1 + \frac{C_s}{C_{ins}}) \frac{kT}{q} \ln 10$$

m **less than 1** ***n*** **less than (kT/q)ln10**

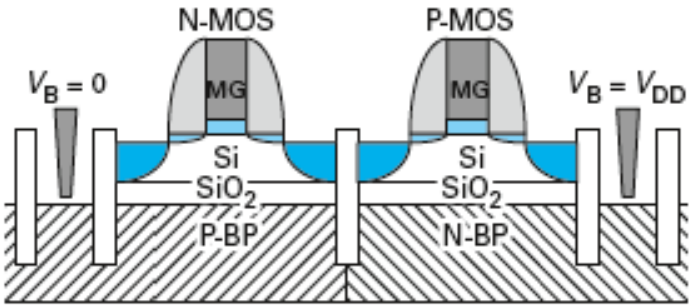
⇒ Decrease of the transistor body factor **m**: **UTB/MG/NW/CNT/Graphene/2D (m~1)** or **m<1**: **NC-FET with Fe materials, MEMS/NEMS …**

⇒ Reduction of **n**: modification of the **carrier injection** mechanisms (or ***low T°*****):**
I.I. (*high V*), BTBT with novel materials …

Advanced bulk & **FD-SOI** MOSFETs:
Scaling (td), Power (S) & Performance (μ)



ⓐ MOS Si



ⓑ SOI

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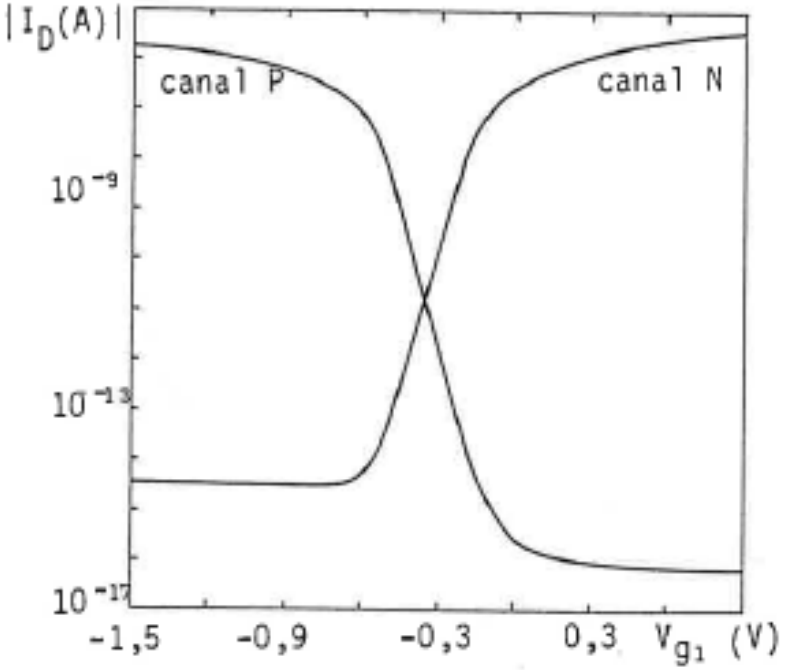
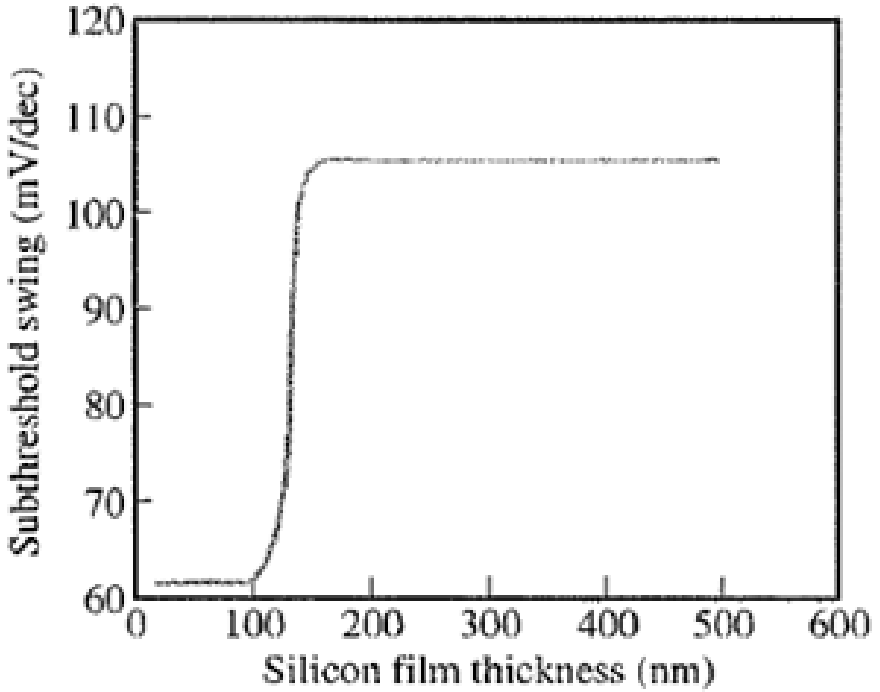
Subthreshold swing of FD SOI MOSFETs

⇒Down to 60mV/dec for UTB at 300K

*1st deep depleted SOI MOSFET, F. Balestra, ESSDERC'**1984** & SSE **1985** & PhD **1985,** JP. Colinge EDL **1986***





60 mV/dec numerical simulation (Balestra PhD'85)

60mV/dec experiment (Colinge EDL'86)

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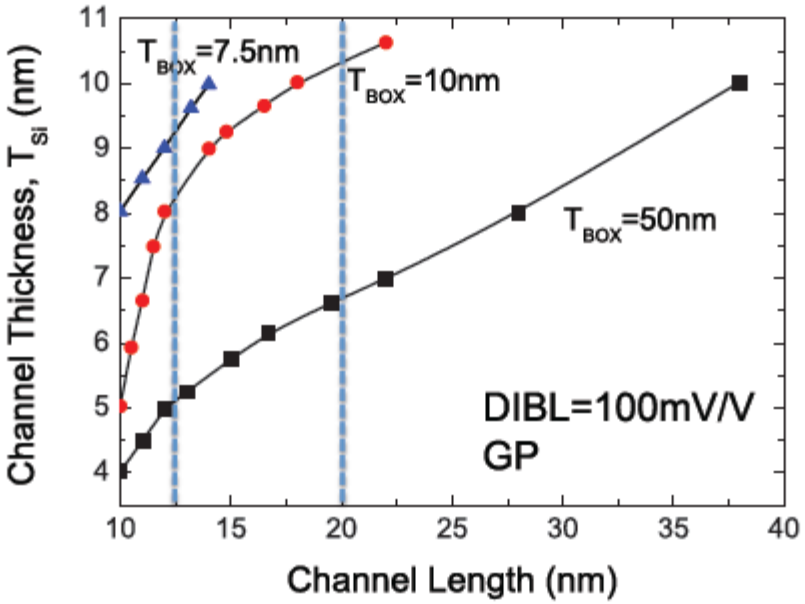
Impact of ultra-thin BOX on FD SOI DIBL and leakage

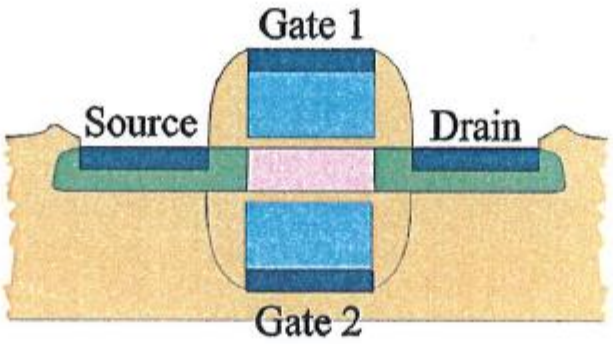
Channel thickness necessary to have a DIBL of 100mV/V as a function of channel length



[F.Andrieu et al., VLSI 2010]

Multi-gate for very low power and HP:
Scaling (td, n), Power (S) & Performance (μ)

Very thin Si,
Ge or III-V film



High-k gate oxide
& metal stack

Double-
or multi-gate

Silicide Schottky
barriers

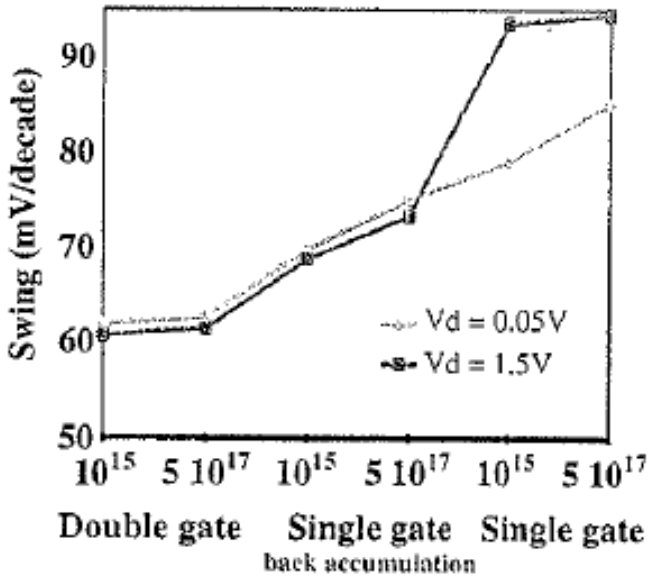
=> Fully Inverted MOSFET (Balestra EDL'**87**)

Subthreshold swing in double-gate SOI MOSFETs

E. Rauly, SSE vol. 43, 1999.

Numerical simulation of subthreshold swing for various types of extremely thin (tsi = 10 nm) SOI MOSFETs (Lg = 0.05 μm)

Single gate
(t_{ox1} = 3 nm and t_{ox2} = 0.38 μm),
double gate
($t_{ox1} = t_{ox2}$ = 3nm),
various dopings
(Na = 10^{15} cm^{-3} and Na = 5 10^{17} cm^{-3})



→ Improvement of the swing : - with reducing the Si film doping
- with a back gate accumulation (Vg2 = -40 V)
- for a double gate SOI MOSFET with volume inversion

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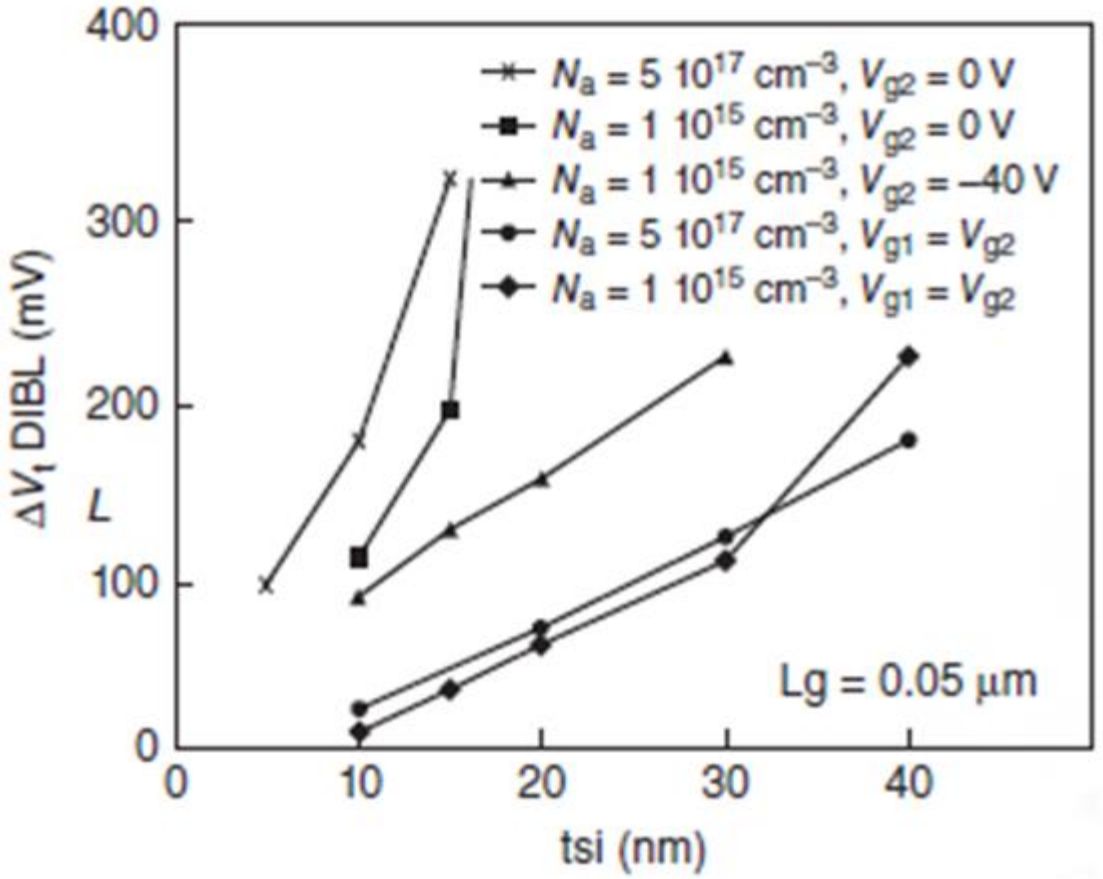
DIBL versus device architecture: 1G, 2G



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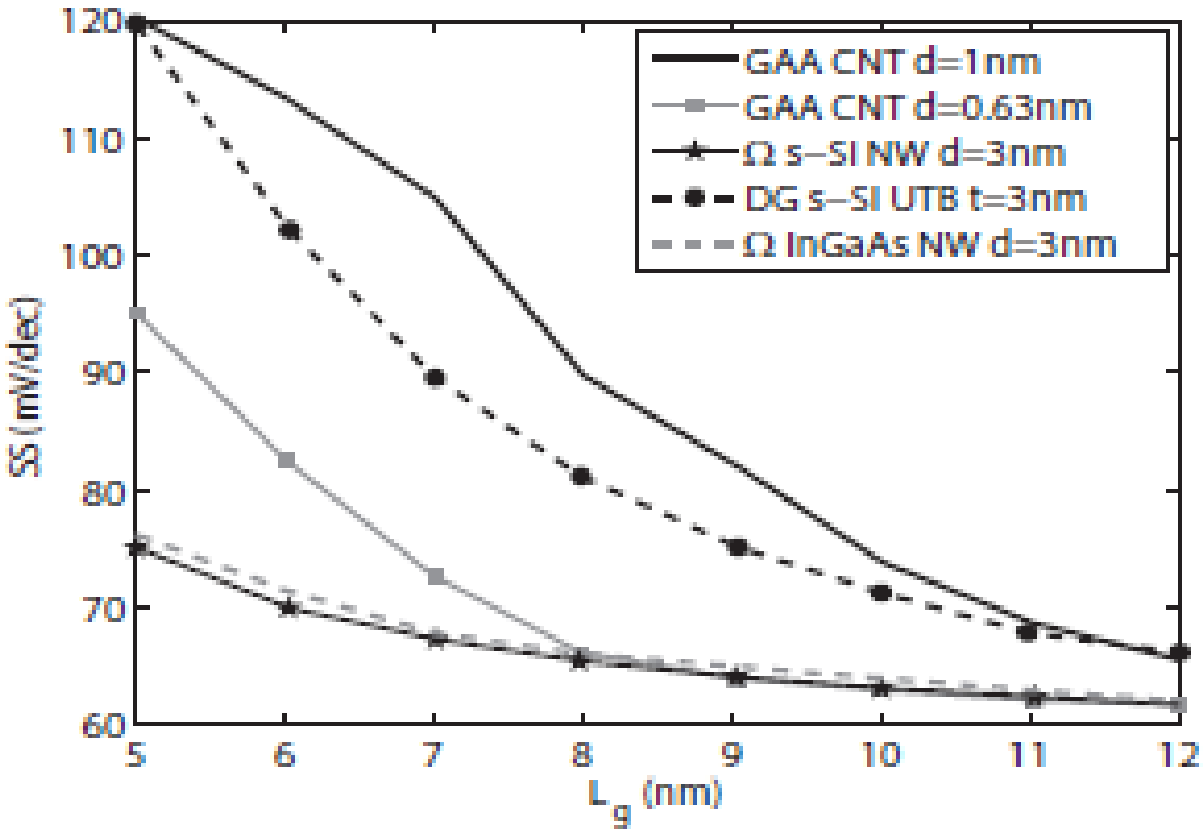
Comparison of S for sub-10nm Lg for:

***Ω-gate sSi** and InGaAs NW, GAA CNT (≠d), DG sSi UTB*

Very good S down to 5nm Lg, but…. >60mV/dec !



(simul. M. Luisier, IEDM11):

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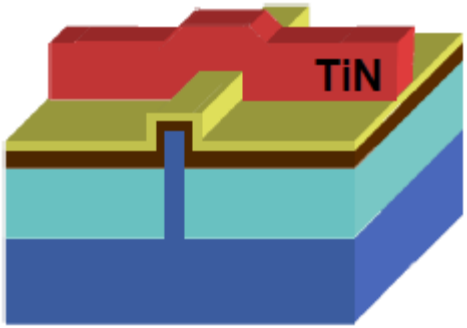
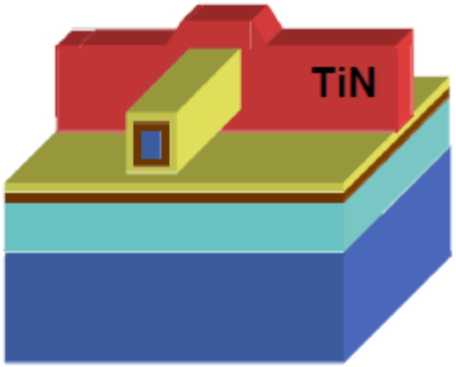
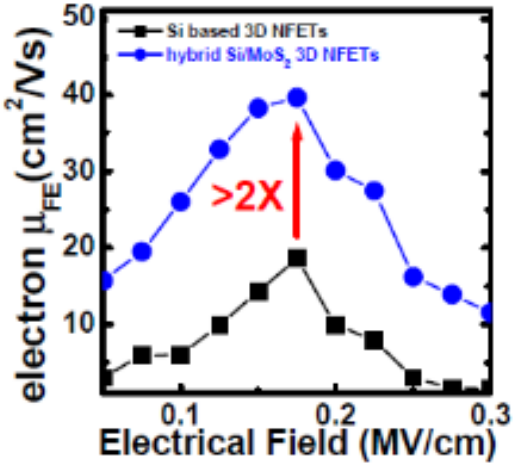
Hybrid Si/TMD Using Solid CVD Few-Layer-MoS2 Stacking

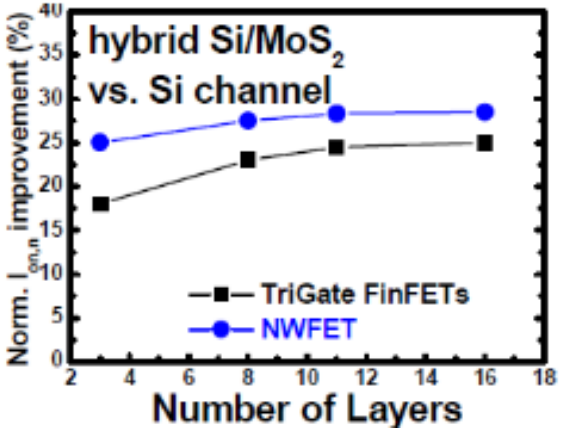
Min-Cheng Chen, IEDM 2014





Si/MoS2/Hf02/TiN Hybrid **FinFET and NW**





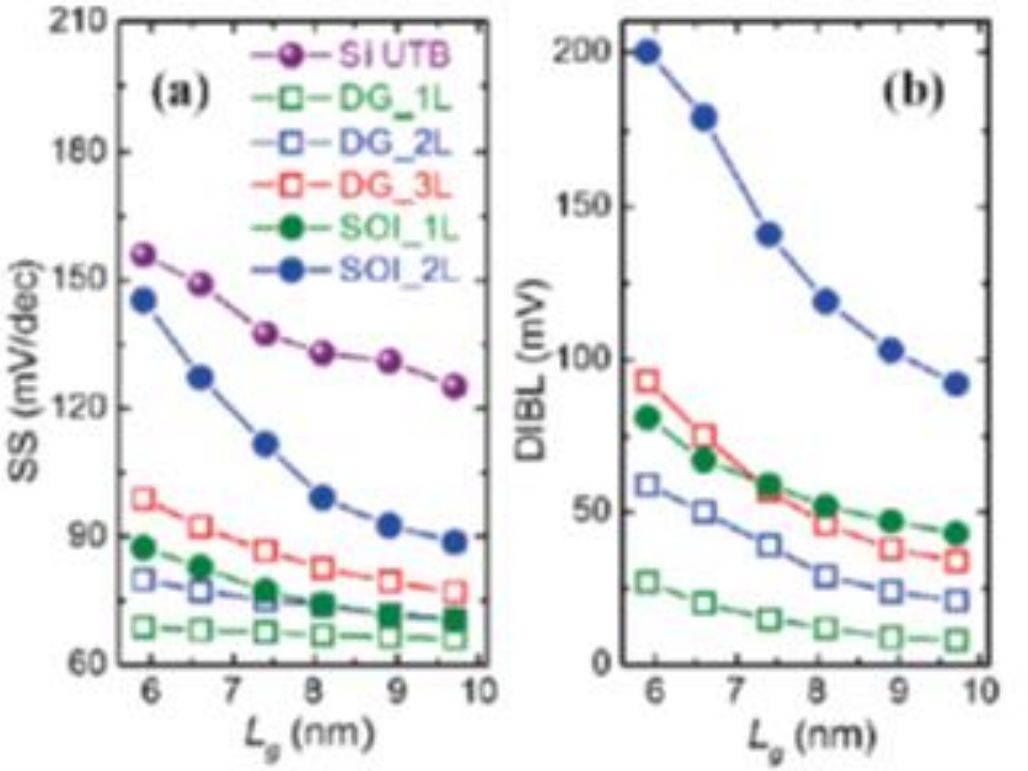
μ ↗ in Si/MoS2 vs Si FinFET

(but need to be evaluated at given Ioff)

Id ↗ in FinFET & NW for Si/MoS2

MoS2 with 1G SOI and DG with 1-3 layers vs Si UTB DG MOSFETs (simul.)

W. Cao, IDEM 2014



Best S and DIBL for DG MoS2 (1L)

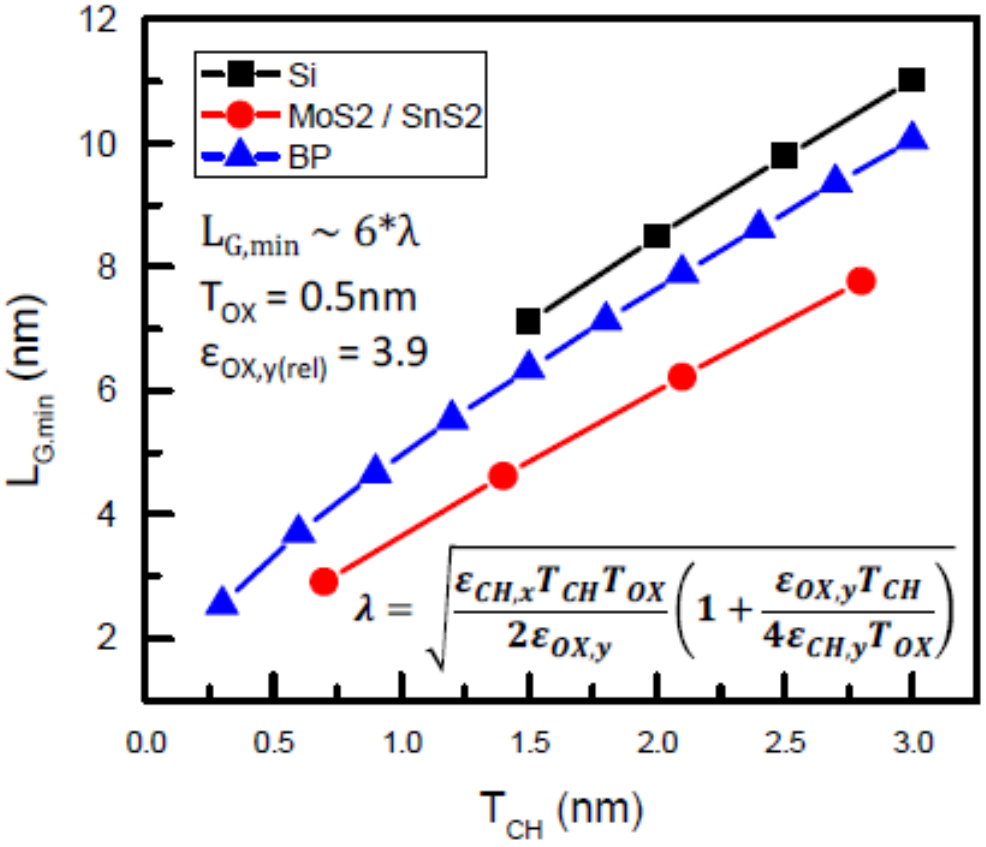
But similar as sSi *Ω-gate* NW with d=3nm

Also need good Nit control

IMEP-LAHC

Comparison of scaling limit for TMDs, Phosphorene/BP and Si

(Modeling, *P. Zhao - IEDM'15*)



Lgmin vs Tchannel for 2G Si (ϵ=12), BP (ϵ=9, Tch=0.3N), TMDs (ϵ=4, Tch=0.7N)

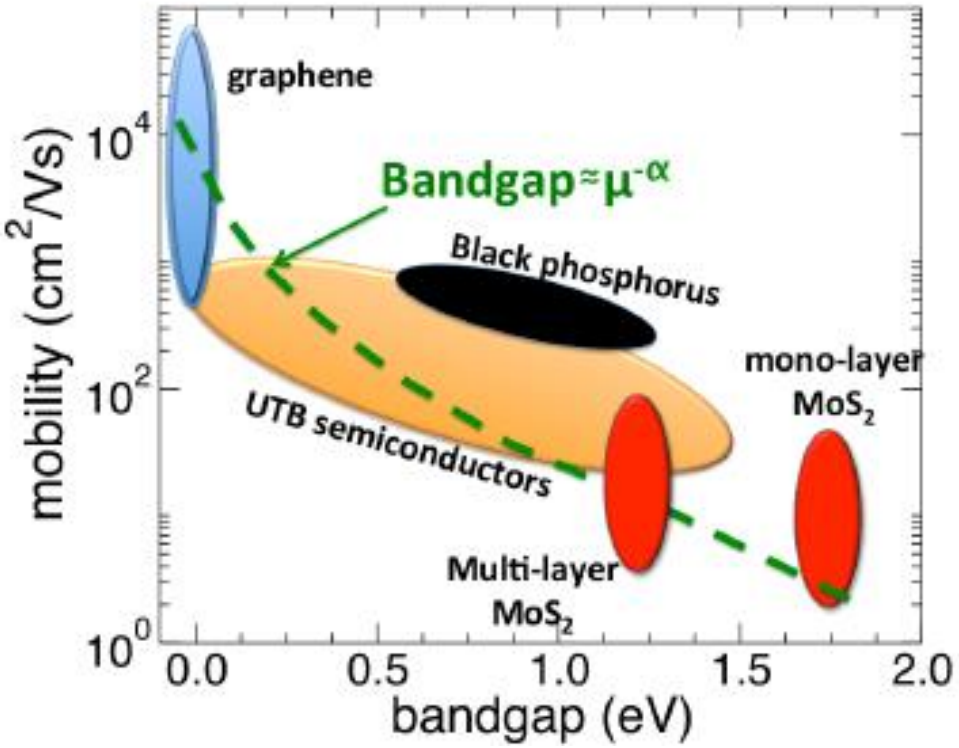
=> Best for TMDs / BP

(N=nb of layers, ϵox=4)

(Rem: high effective mass along the channel for 2D materials => S-D tunneling could ↓ / Si for sub-5nm Lg)

Mobility vs bandgap for various 2D materials and UTB semiconductors

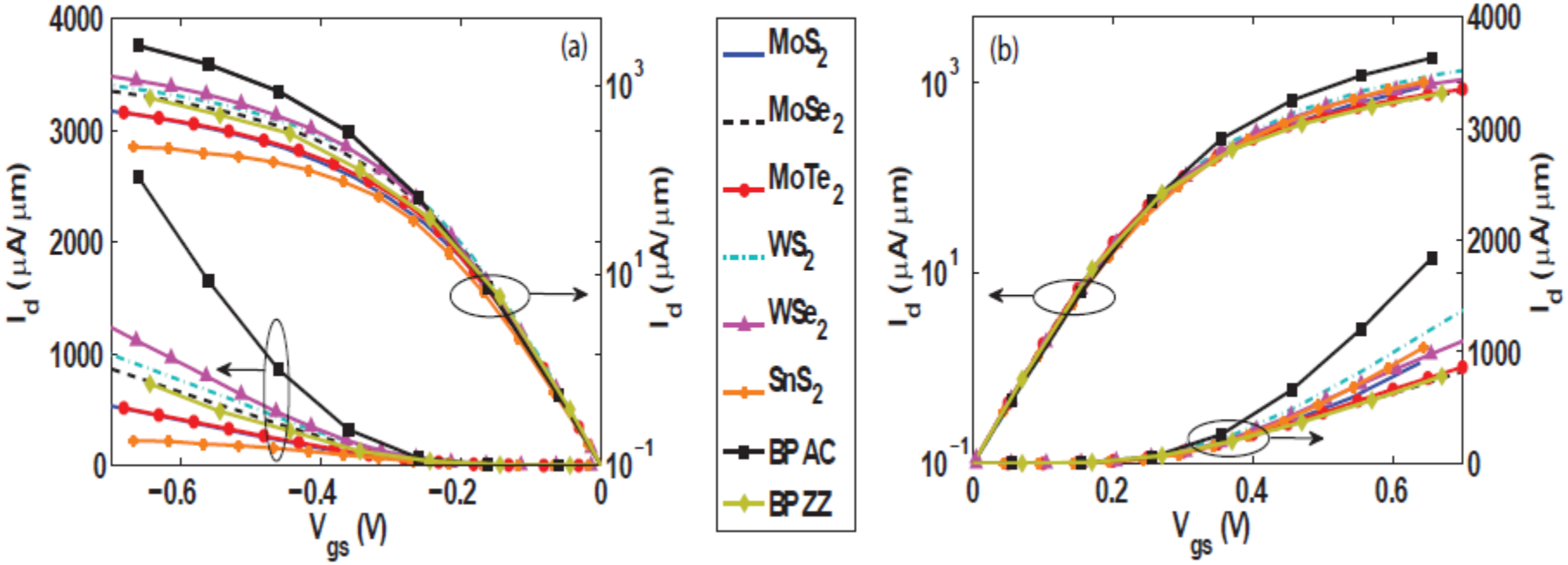
(*G. Fiori - IEDM'15*)



μ ↗ when bandgap ↓

BP good trade-off but many technological issues

Ab-initio simulation of 2D MOSFETs

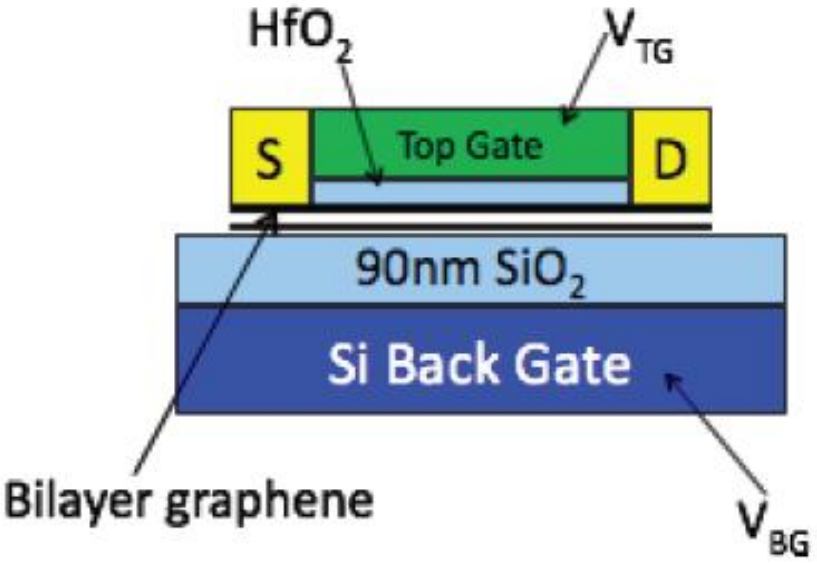


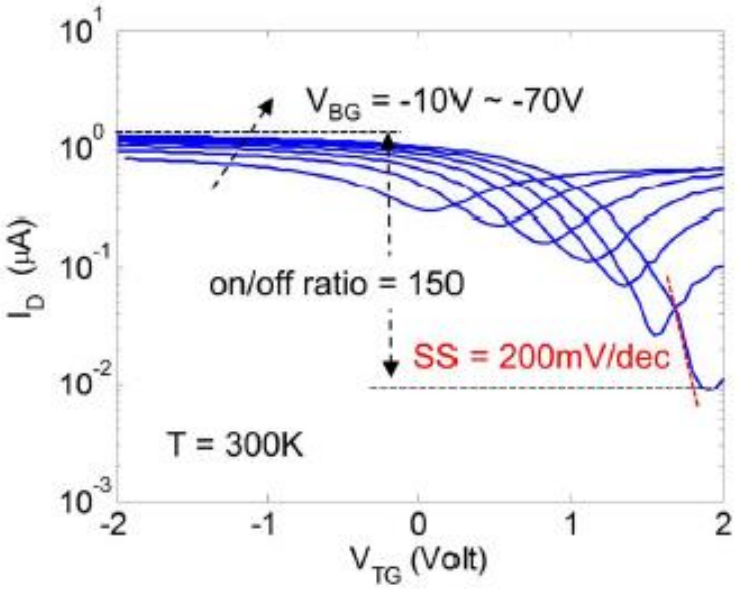
Best Idon for Black Phosphorous (AC: transport parallel to the armchair configuration) for n and p devices compared to several TMD channels (no Rsd)

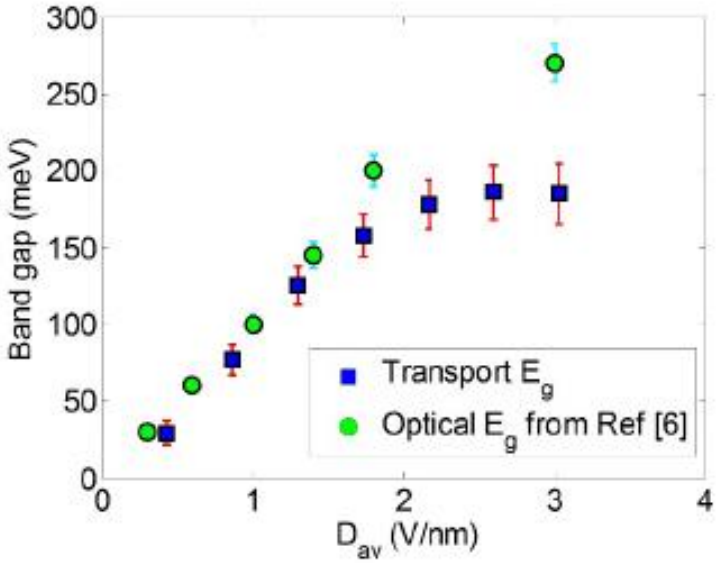
M. Lusier, IEDM 16

Bandgap engineering in 2D materials by Electric field: Graphene

(Experimental, *T. Chu - IEDM'15*)



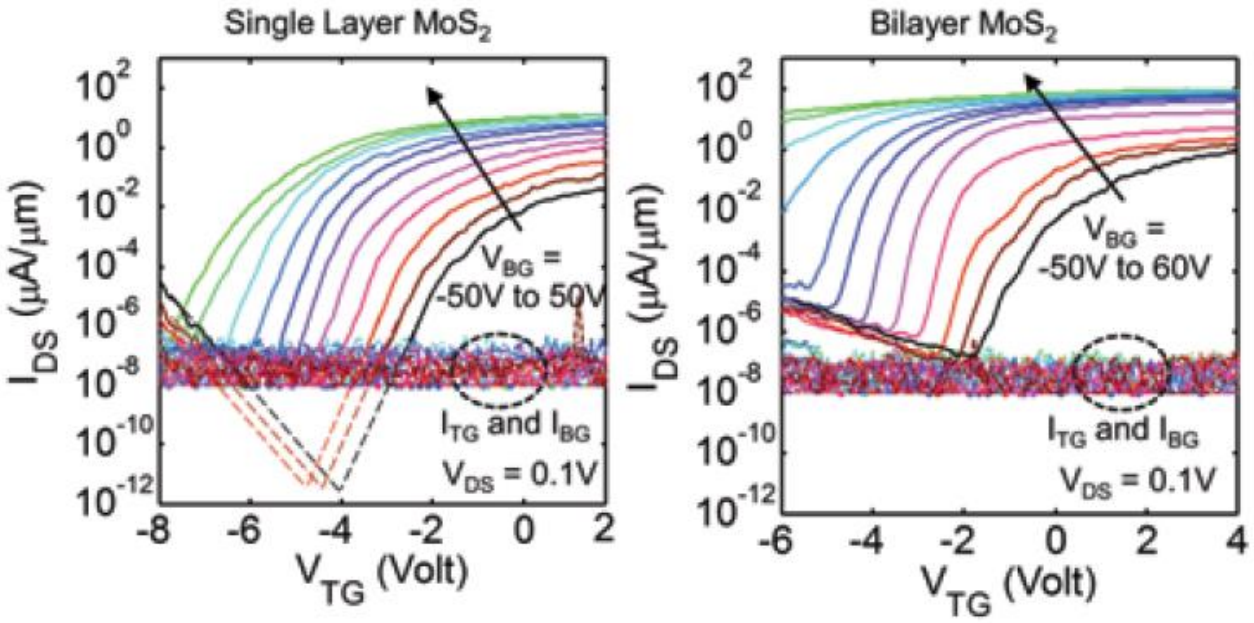




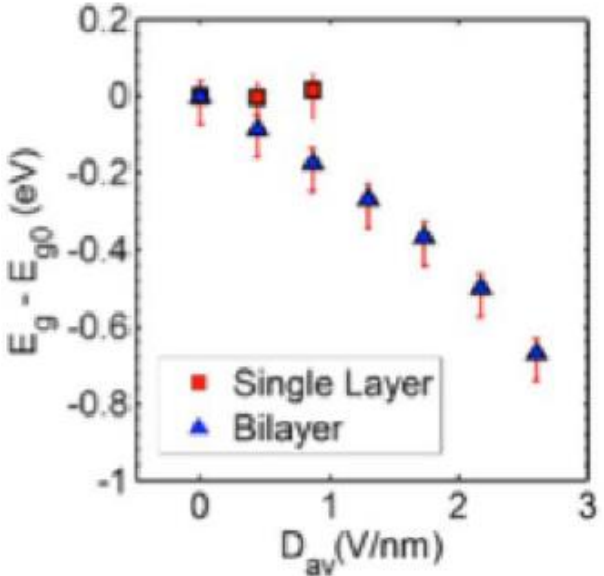
Ion/Ioff and Bandgap ↗ in Bilayer Graphene Ribbon (100nm) with transverse Electric Field (front 7nm HfO2 and back gate)

Bandgap engineering in 2D materials by Electric field: TMDs

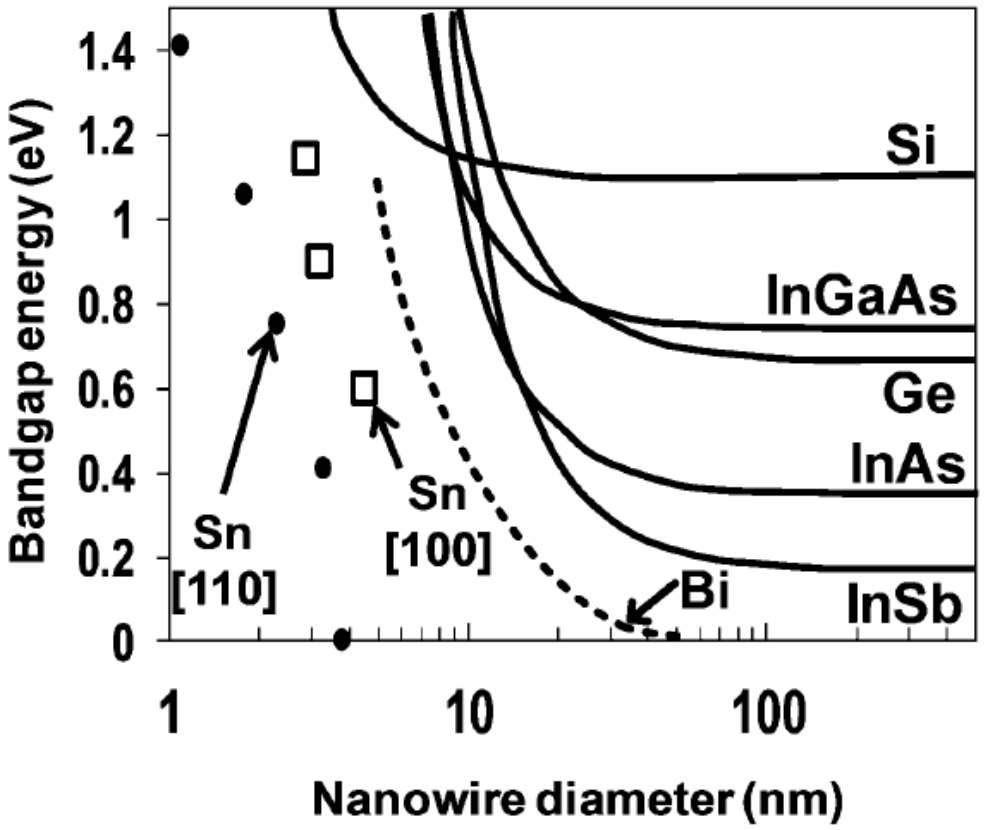
(Experimental, *T. Chu - IEDM'15*)



Bandgap and Ion/Ioff↓ when Vgb ↗ for Bilayer MoS2 inducing a Semi-Metallic state



Bangap in 1D structures



Ansari, Nano Letters 2012

Bangap ↑ when NW diameter ↓ for Semiconductors and Semimetals

=> Semimetal -> Semiconductor

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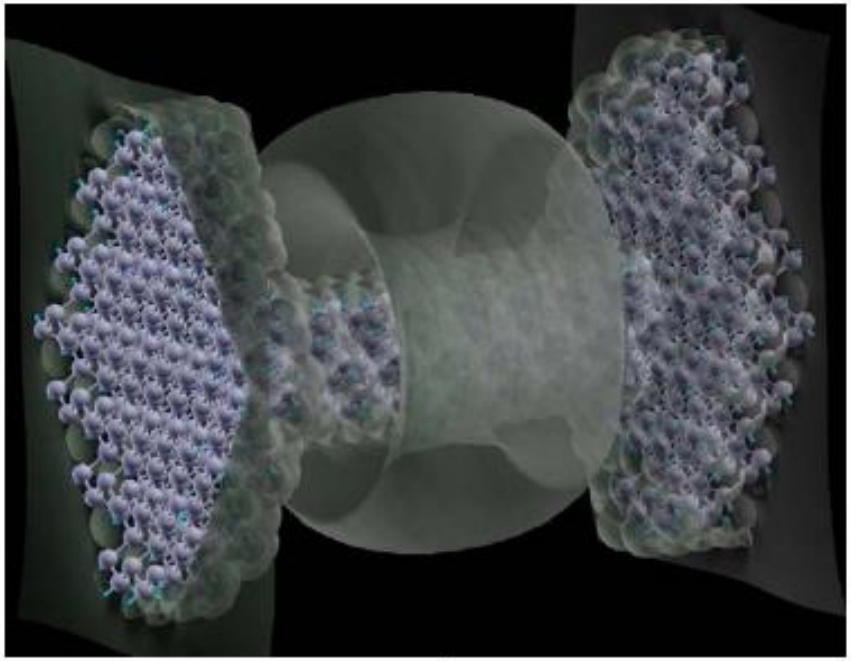
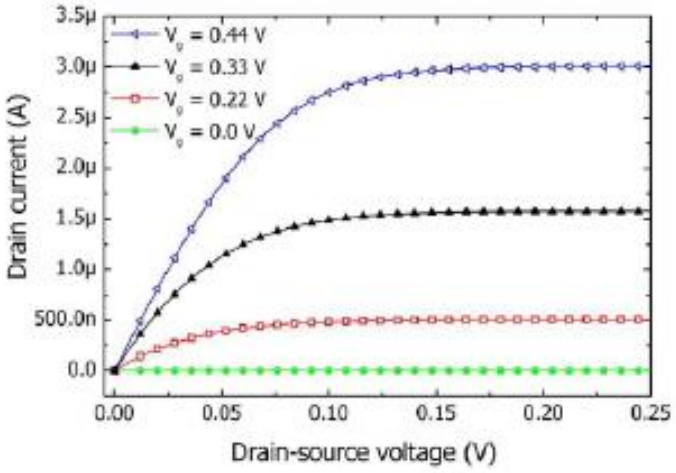
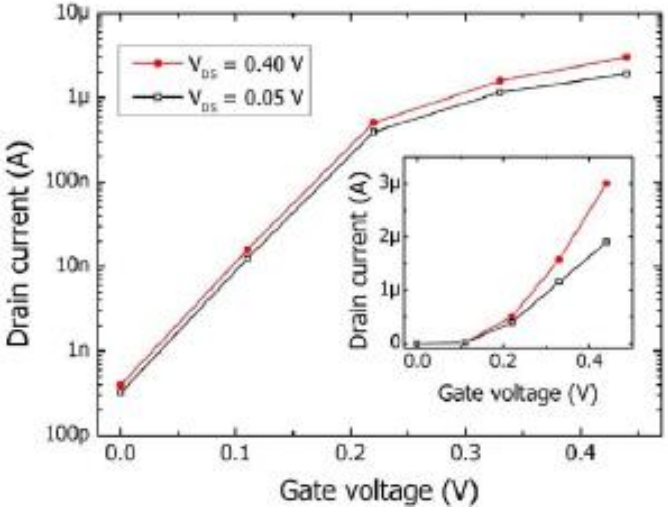
Example: Sn NW (Ab-initio simulations)



L = 2.3 nm, Ø = 1 nm
Subthreshold Slope=72 mV/dec
I_{on} = 3000uA/um @V_{DS}=250mV





⇒ ***No doping in channel and S/D***

⇒ ***Very good result but very small d needed <2nm for same Eg as Si (similar as graphene nanoribon)***

⇒ ***Need very good d control*** *(variability)*

Ansari, Nano Letters 2012

Solutions for reduction of S below 60mV/dec

-Strong reduction in Vdd and Emin possible using new physics/materials/devices with **sub-60mV/dec subthreshold swing** (*limit of MOSFETs at RT*):

⇒ **Energy filtering**: *Tunnel FET* (MOS- NW- CNT- or Graphene-based): BtB tunneling to filter energy distribution of electrons in the source (cuts off the high energy e/Boltzmann tail resp. for 60mV/dec): **PB => Ion**

⇒ **Internal voltage Step-up**: *Ferroelectric gate FET* (inducing a negative capacitance to amplify the change in channel potential induced by the gate): **PB => long switching times**

⇒ **NEMS/NEMFET/relay: PB => voltage scaling, reliability**

⇒ **Hybrid devices:** Fe TFETs, Phase Change materials, Atom Scale filament…

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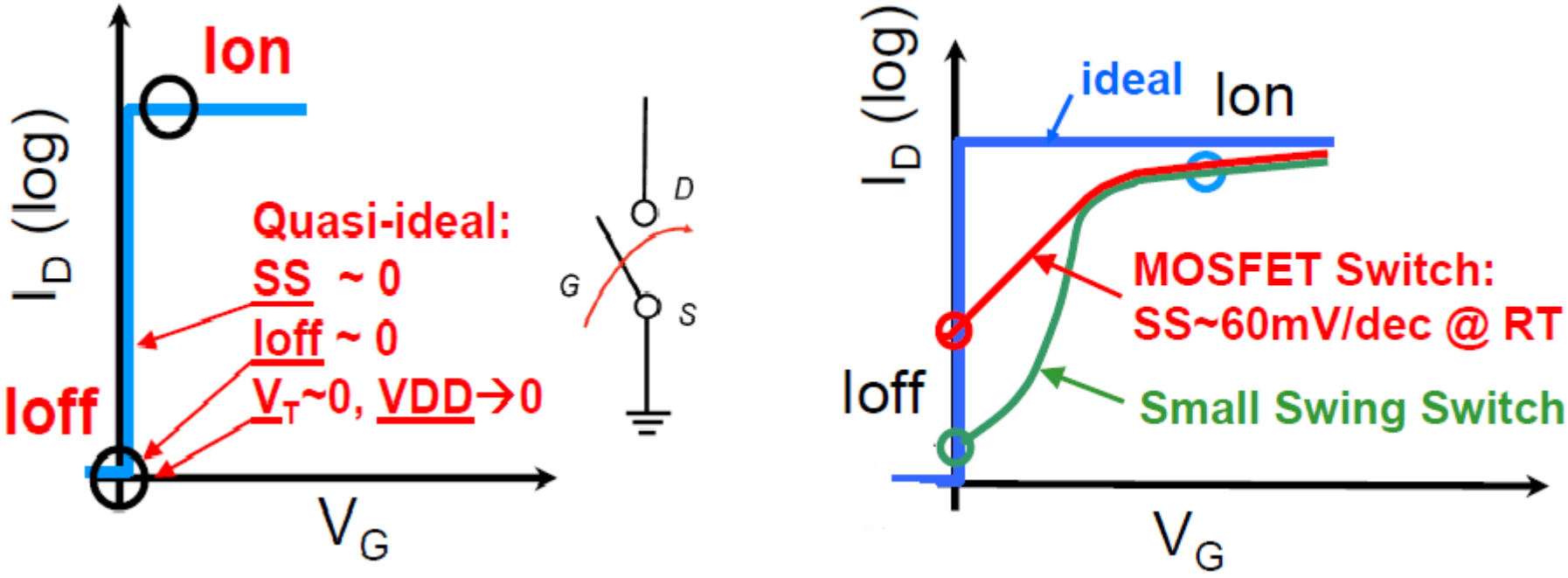
The quasi-ideal switch



- *Quasi-ideal binary switch:*

  - 2 stable states (off, on)
  - Ion: as high as possible
  - Ioff: as low as possible
  - abrupt swing (mV/decade)
  - very fast (<ns)

Small swing switch best parameters

To outperform CMOS:

-Ion: range of hundreds of µA

-S_{avg} far below 60mV/dec for at least 4-5 decades of Id

-Ion/Ioff > 10^5

-Vdd<0.5V

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Reduction of S below 60mV/dec: Very promising => *TFETs*

-Very promising ones, **TFETs**, use **gate-controlled pin structures** with carriers tunneling through the barrier and not flowing over:

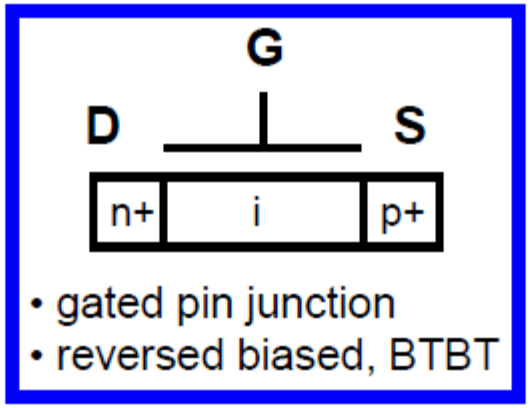
⇒ **Interband tunnelling** in heavily-doped p+n+ junction with a control of band bending with Vg and a reversed bias p-i-n

=> *Ambipolar effect* has to be suppressed by assymmetry in the doping level or profile, or the use of heterostructures

Tunnel FET

OFF-state

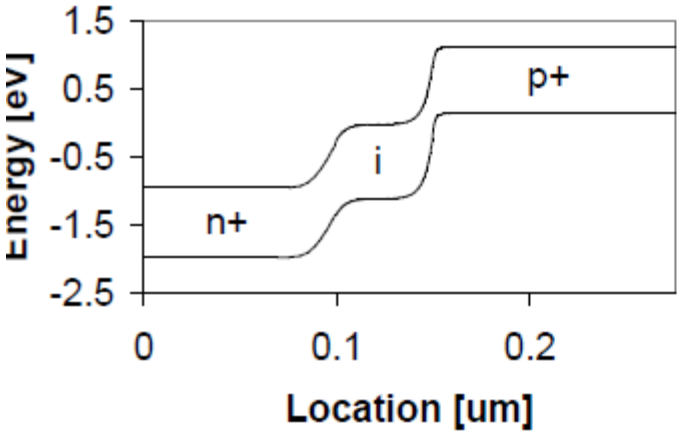
- V_d = positive
- V_g = 0
- **no current flows**

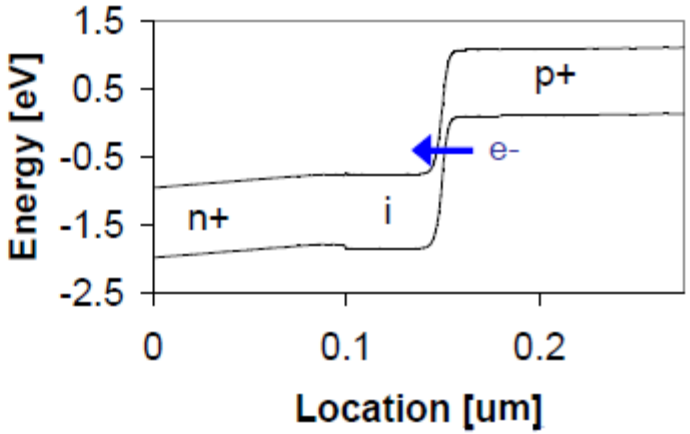


- gated pin junction
- reversed biased, BTBT

ON-state

- V_d = positive
- V_g = positive
- **barrier thin, current flows**





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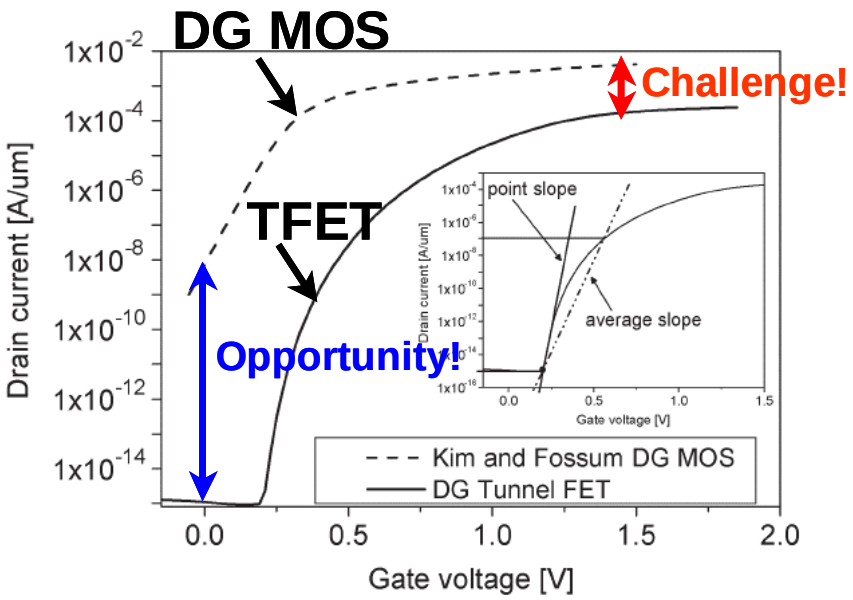
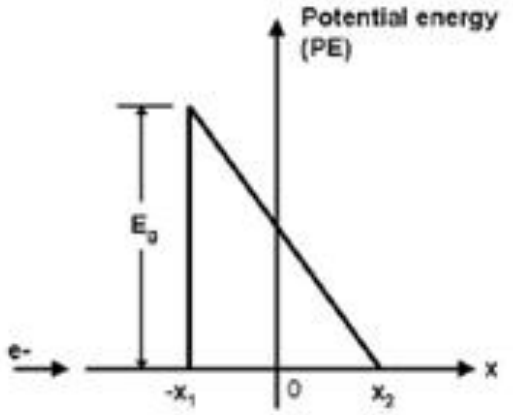
Tunnel FET

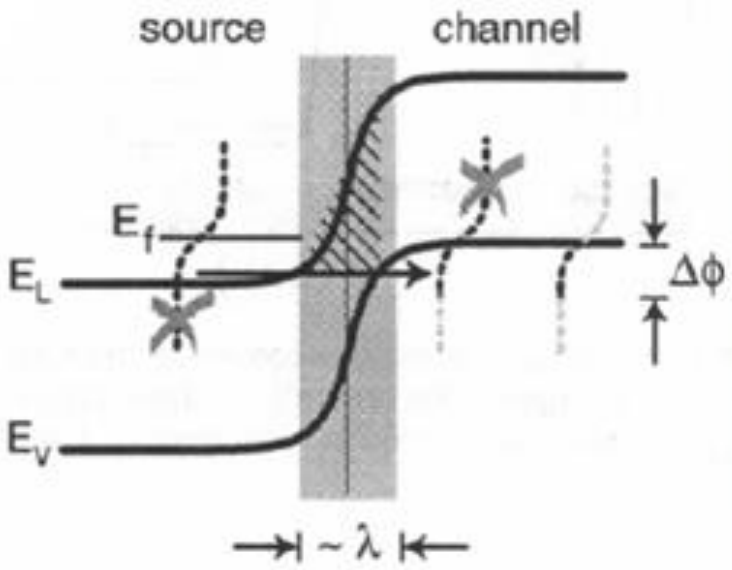
- **Opportunities**: reduce by decades standby power
- **Challenges** for Tunnel FETs:
  - bandgap engineering
  - *on-state* performance improvement needed
  - exploitation of innovative (nano)structures



A.M. Ionescu, VLSI ITRI 2008.

Major parameter for BTBT: Transmission probability



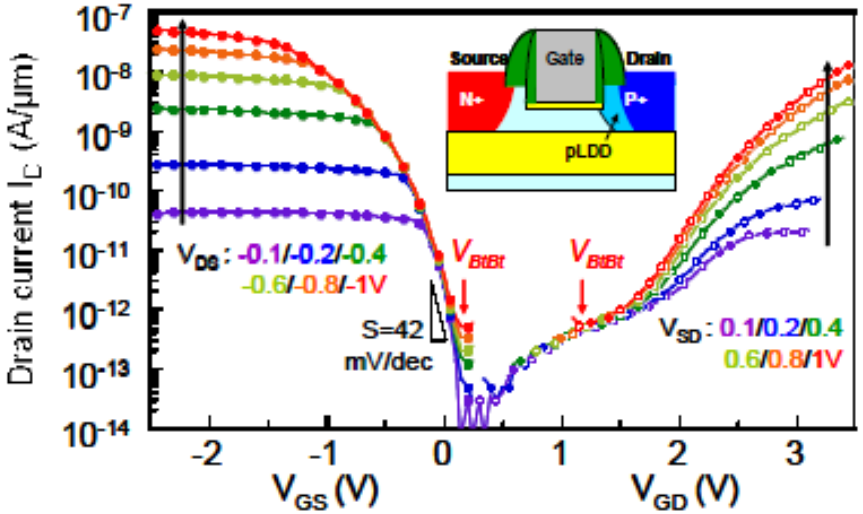


$$I_{BTB} \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{1.5}}{3\eta(\Delta\Phi + E_g)}\right)$$

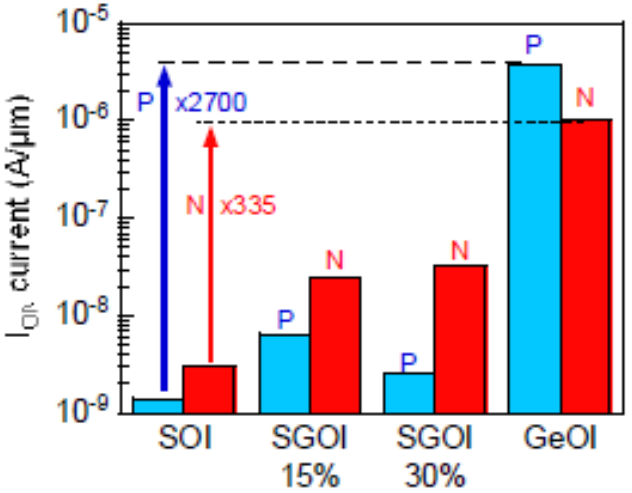
Parameter	Means of improvement
m^*	Small effective tunnel mass, SiGe, III-V, CNT
E_G	Source in SiGe, III-V heterostructures, strain CNT
λ	3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric

Tunnel FET on Si, SGOI, GOI

S=42mV/Dec, Ioff<0.1pA, *but* ***Ion<0.1µA*** *at Vd=1V* (exp.)



$I_D(V_G)$ characteristics of a L_G=100nm SOI TFET in p (left) and n (right) channel operation modes (t_{Si}=20nm; P30: pLDD, 30nm 2nd spacers). Local subthreshold slope at low as 42mV/dec is measured. We define V_{BtBt} as the voltage at which band to band tunneling occurs.



Extracted TFET ON current (at V_{DS}= ±0.8V, V_{GS}= ±2V) for 400nm gate length TFETs on $Si_{1-x}Ge_xOI$ (x_{Ge}= 0-15-30%, t_{SiGe}=20nm), and GeOI (T_{Ge}=60nm) substrates (in p & n modes).

(F. Mayer et al, IEDM 2008)

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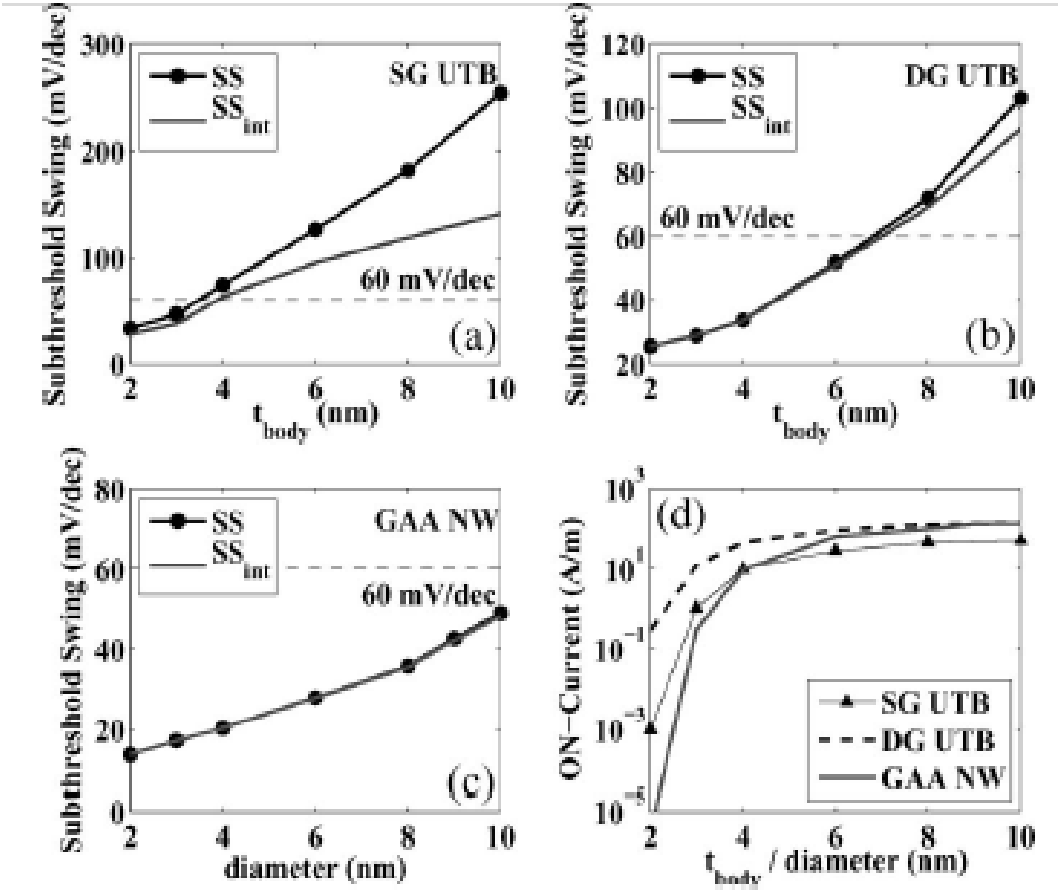
III-V channel TFETs

- * **InAs TFETs (SG, DG, GAA NW):** small bandgap and electron-hole effective masses inducing BTBT (Vg=Vd=0.2V) (*M. Luisier EDL 2009, Simul.)* :



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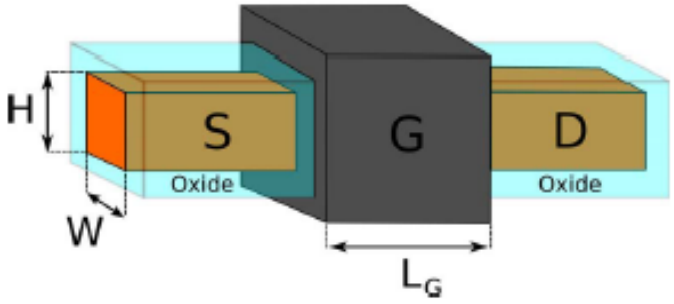
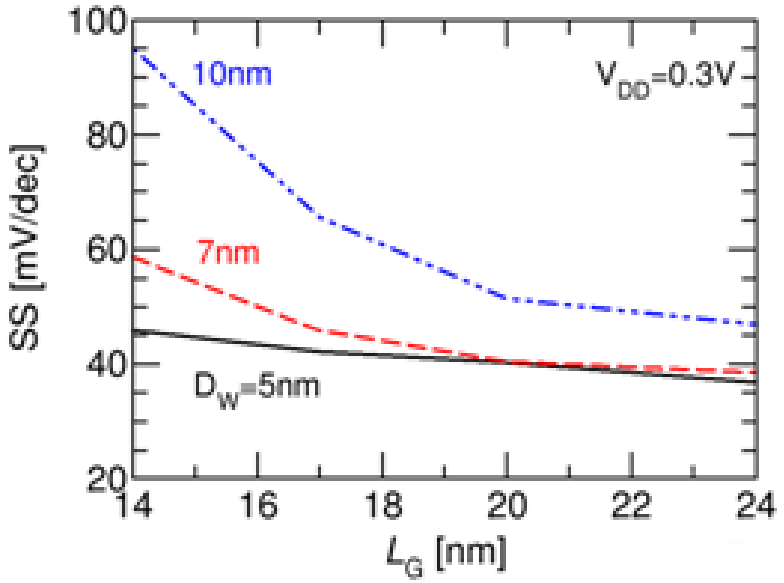
InAs NW TFETs





Subthreshold swing vs gate length for GAA InAs Nanowire TFETs for various wire diameters obtained by quantum simulation

F. Conzatti
IEDM 2011
(3D quantum transport simulation)

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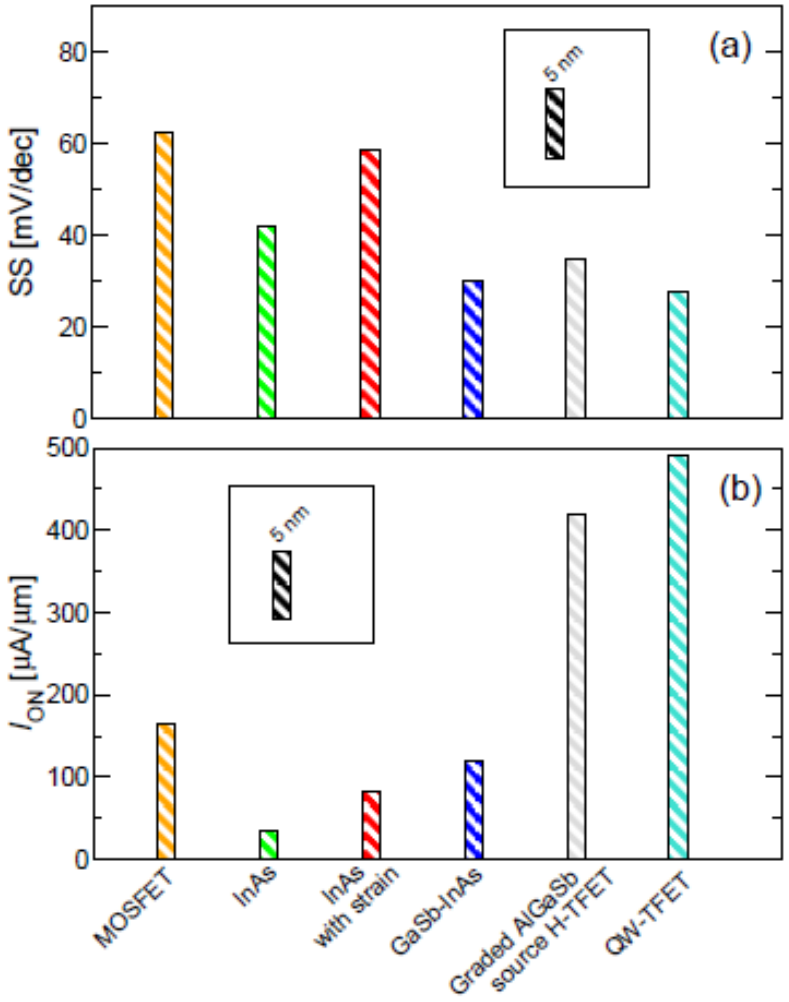
Comparison of all III-V TFET architectures



⇒ **QW-TFET best performance (InAs-GaSb-InAs Qantum Well)**

-Graded source H-TFET with Tgrad=5nm

-Quantum well TFET with Twell =3nm

Dw=5nm, Lg=17nm, Ion at Ioff=5nA/µm

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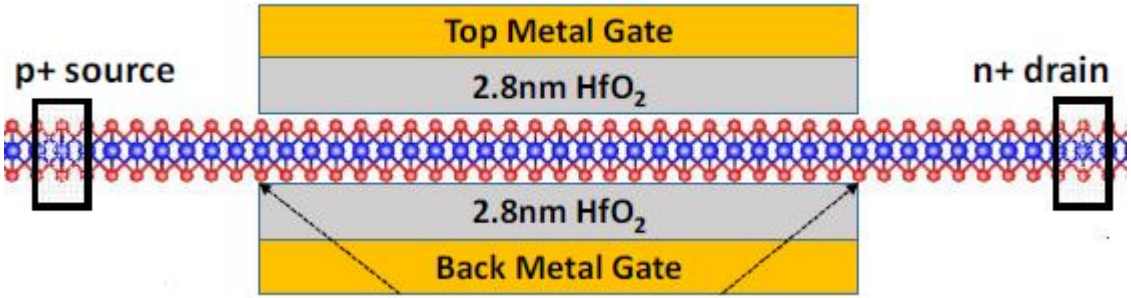
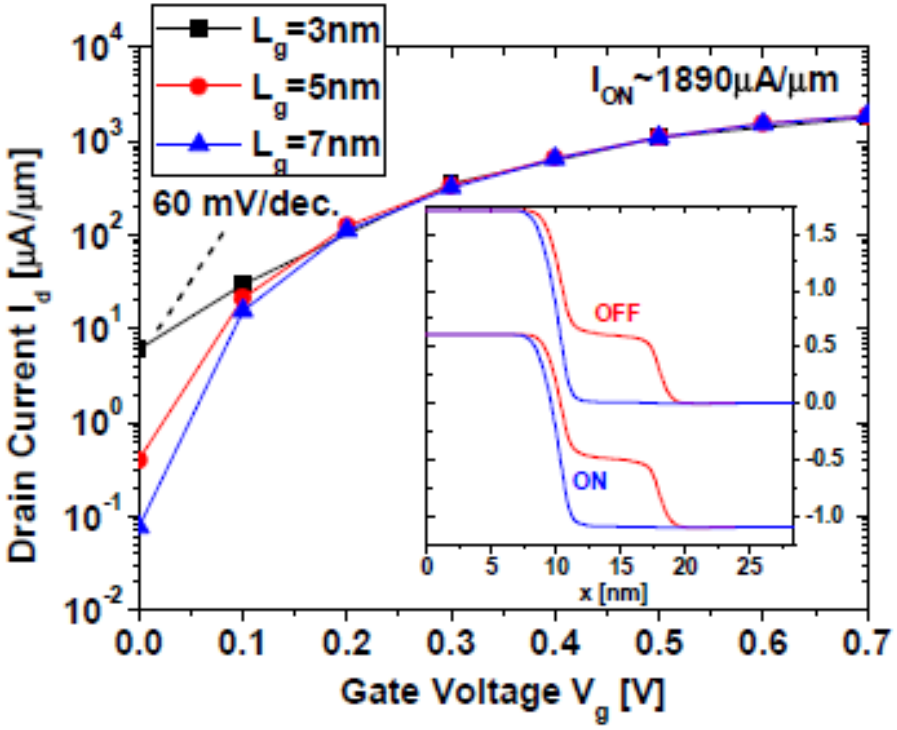
2D/WTe2 TFET

(Ab-initio quantum simulation, *X.-W. Jiang - IEDM'15*)





Best results for TMD layers obtained with **WTe2 TFET** for HP and LOP applications

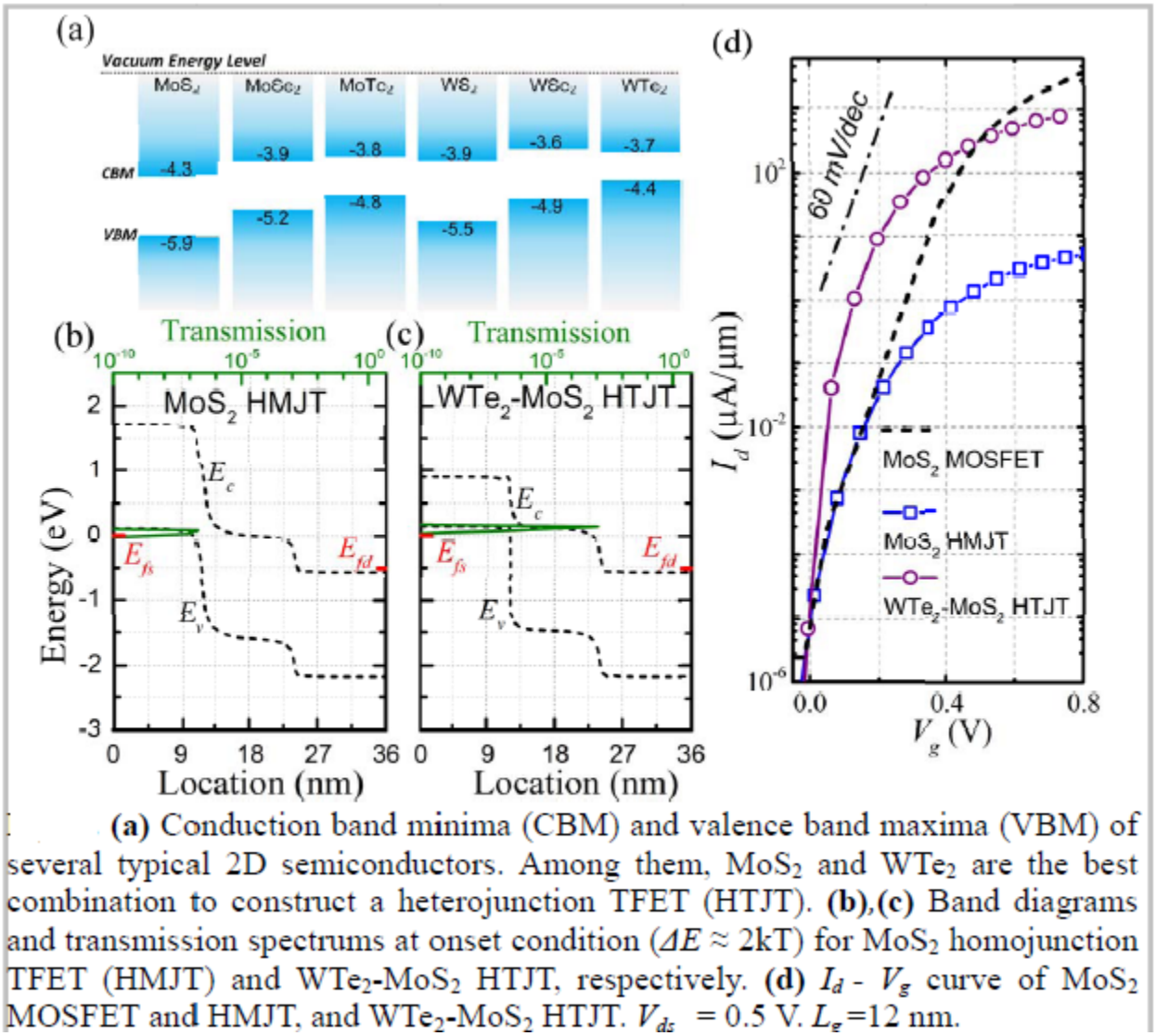
Vd=0.5V, S/D doping $10^{13}cm^{-2}$

Performance for Lg=7nm close to ITRS HP 2024 requirement

Ioff degradation for Lg<5nm

Comparison of Homojunction and heterojunction 2D TFET

(NEGF quantum simulation, *W. Cao - IEDM'15*)

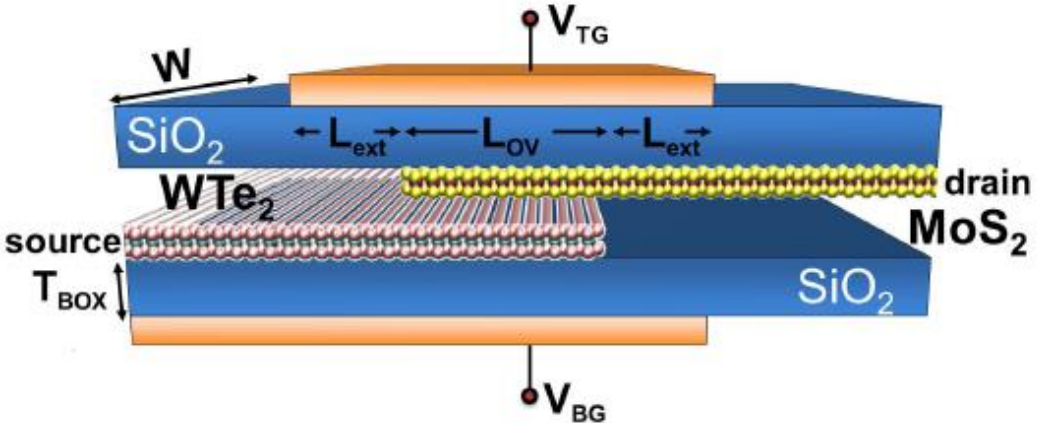


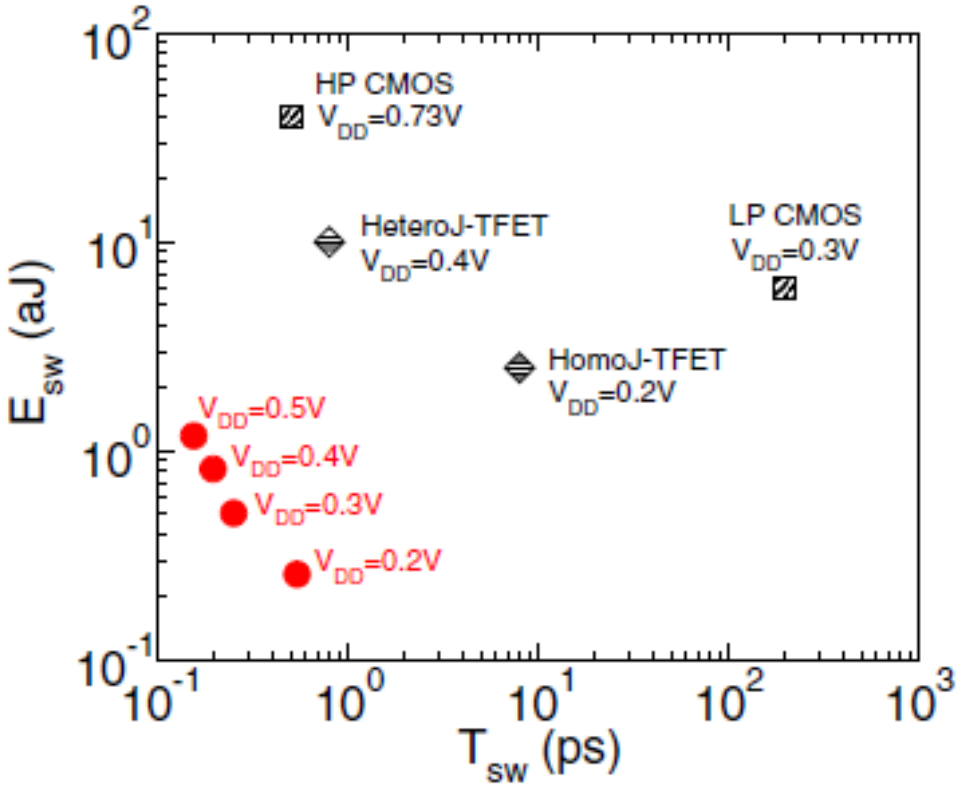
(a) Conduction band minima (CBM) and valence band maxima (VBM) of several typical 2D semiconductors. Among them, MoS_2 and WTe_2 are the best combination to construct a heterojunction TFET (HTJT). **(b),(c)** Band diagrams and transmission spectrums at onset condition ($\Delta E \approx 2kT$) for MoS_2 homojunction TFET (HMJT) and WTe_2-MoS_2 HTJT, respectively. **(d)** I_d - V_g curve of MoS_2 MOSFET and HMJT, and WTe_2-MoS_2 HTJT. V_{ds} = 0.5 V. L_g=12 nm.

Best results for
Heterojunction
WTe2-MoS2 TFET

2D (MoS2-WTe2) TFET

(Quantum simulation, *J. Cao- IEDM'15*)



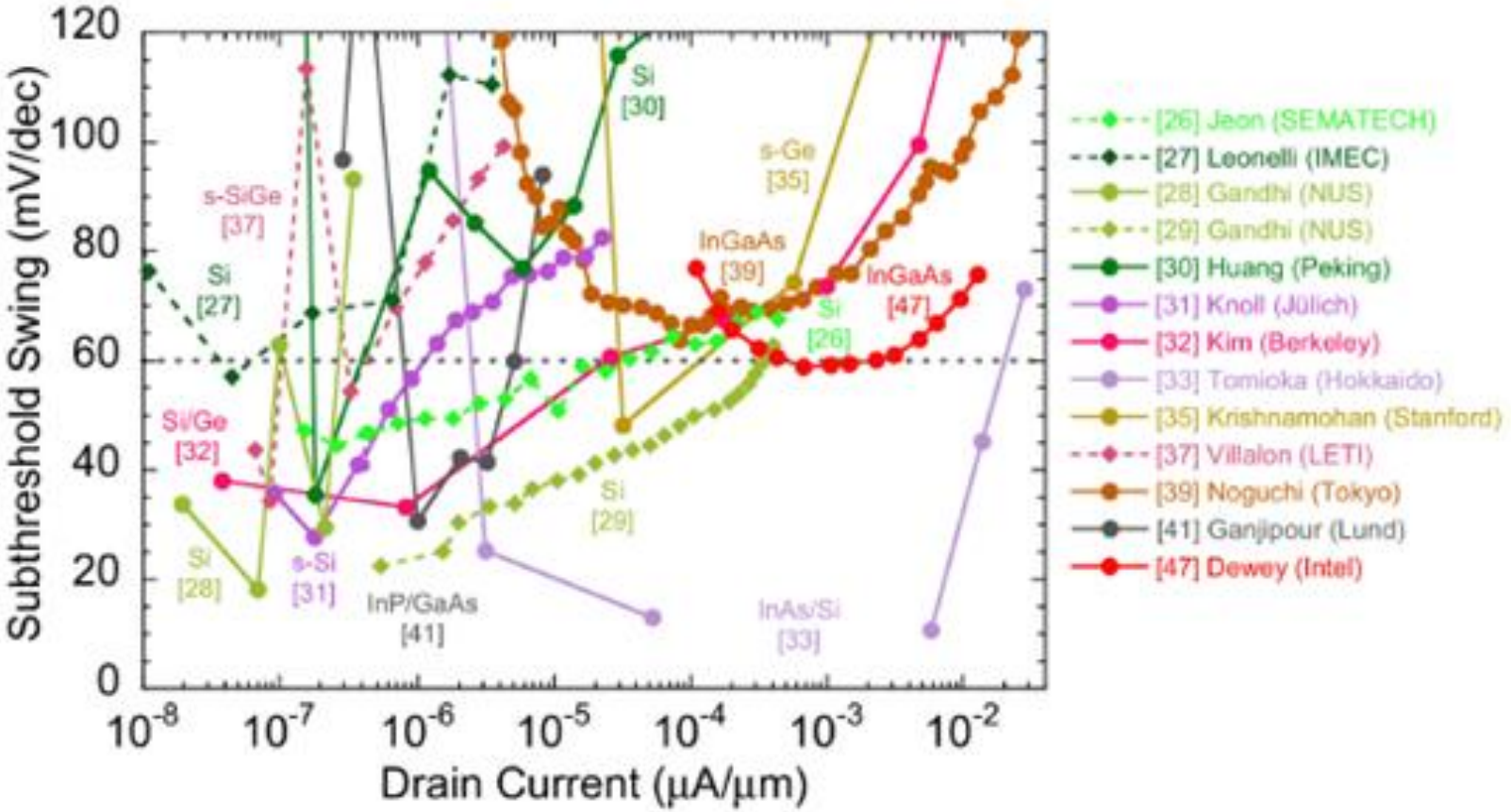


Intrinsic switching energy vs Switching time for various devices : CMOS, TFET (InAs and InAs/GaSb) and **2D TFET MoS2-WTe2** (**best results**)

Front and back SiO2, 0.35nm gap with ϵ=1, chemically doped MoS2 ($4.10^{12}cm^{-2}$) and electrostatically doped WTe2 with Vbg

Comparison TFET experimental results (<2016)

H. Lu, J. Electr. Dev.Soc. 2014



⇒ S < 60 mV/dec for Id < 10 nA/μm

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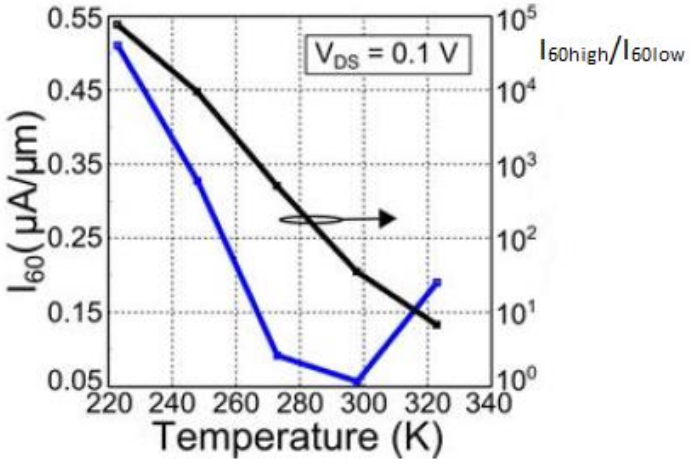
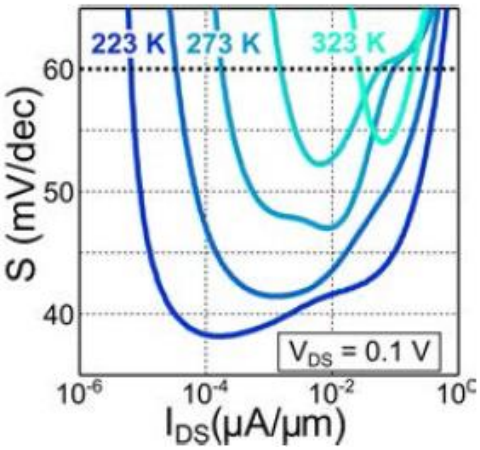
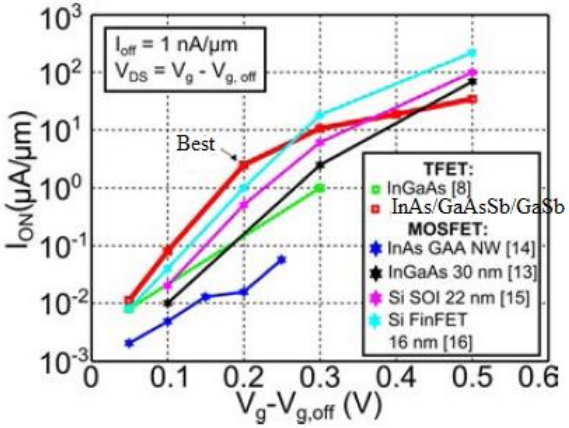
Vertical InAs/GaAsSb/GaSb NW TFET







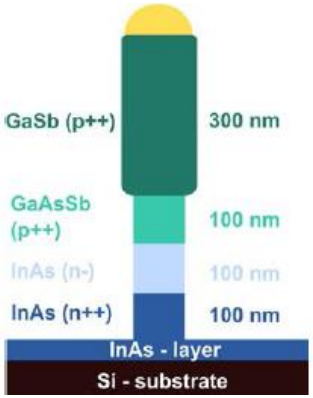
-I_{60} is 0.056 μA/μm and **0.31 μA/μm**

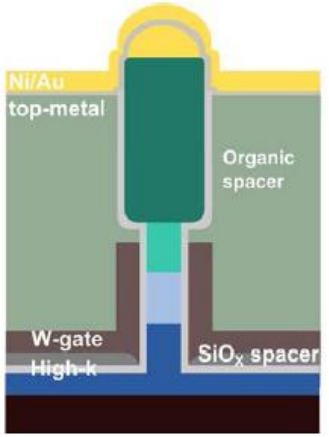
at VDS = 0.1 and ***0.3 V*** (record exp.)

-Smin~50mV/dec at 300K

-Best Ion for Vg<0.25V

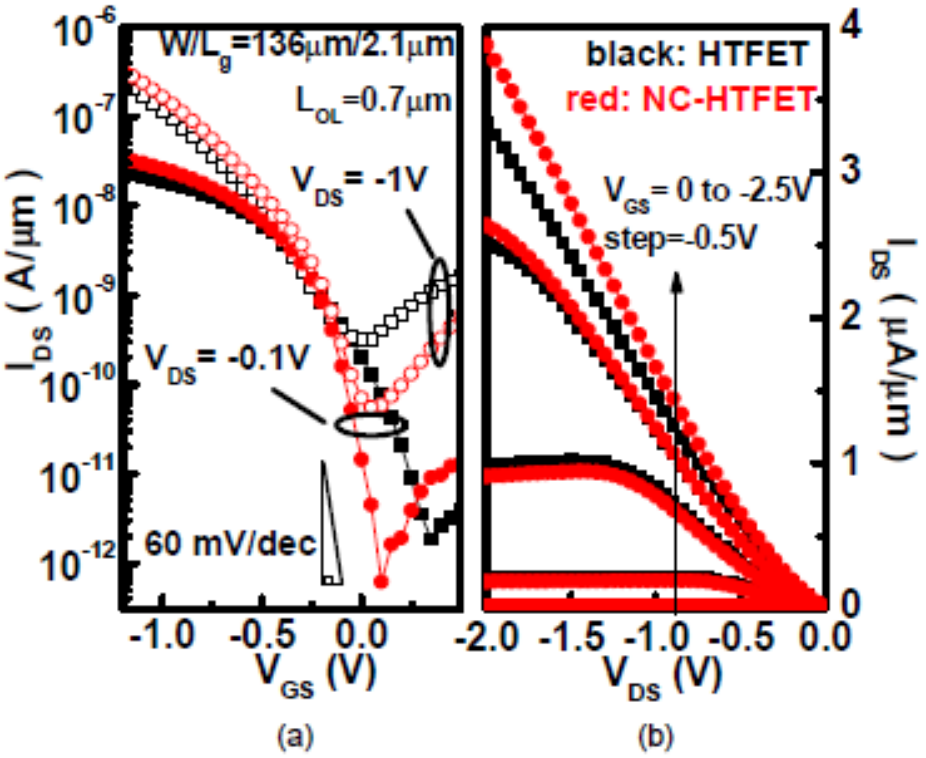
(d=20nm, Lg~100nm)



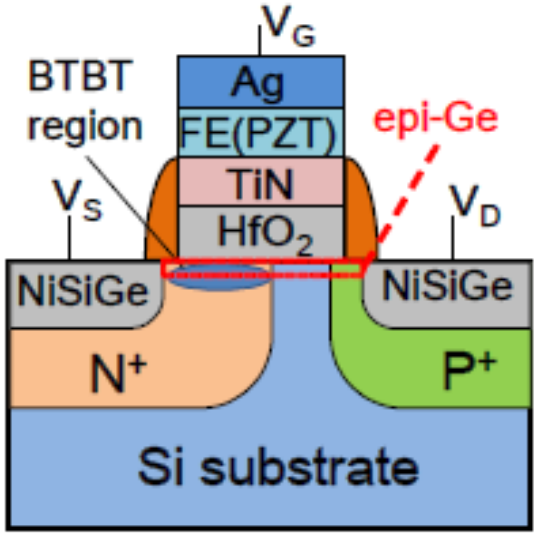


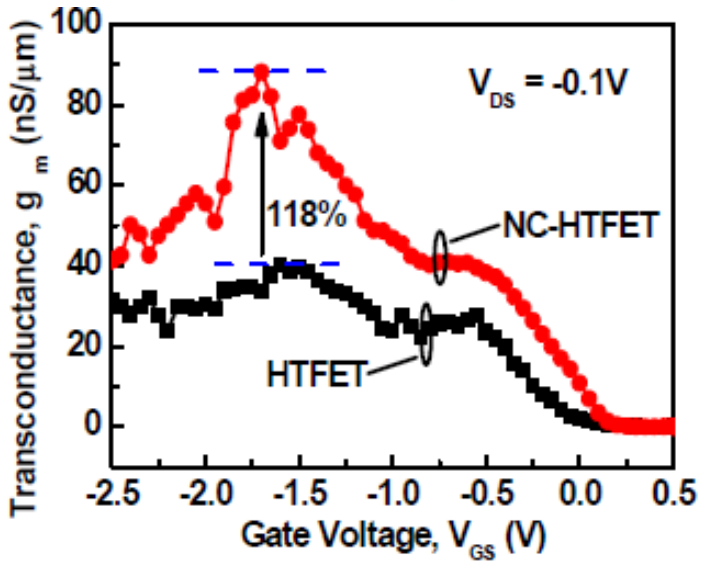
E. Memisevic, IEDM 16

Hybrid device:TFET-FeFET



(a) Transfer characteristic (b) Output characteristic of NC-HTFET. The subthreshold swing is improved significantly with NC. The current of NC-HTFET shows the enhancement with larger V_{GS}. Note that both HTFET and NC-HTFET are the same devices for comparison.



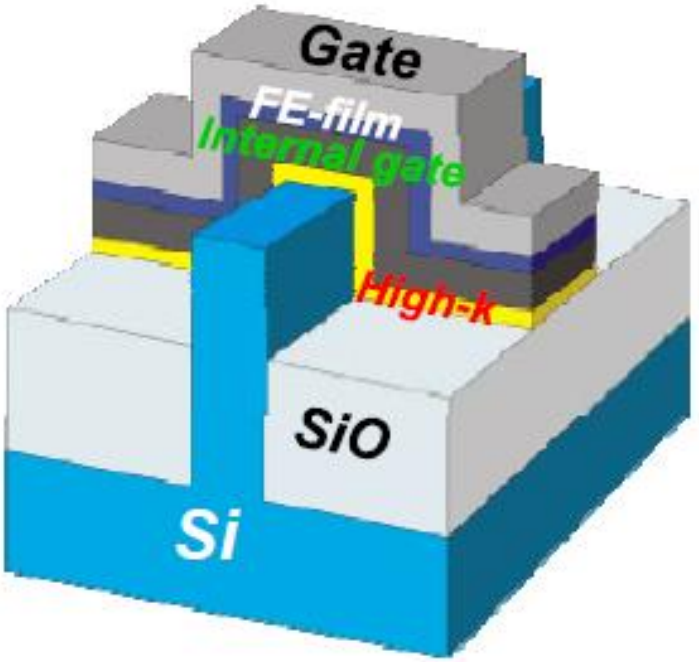


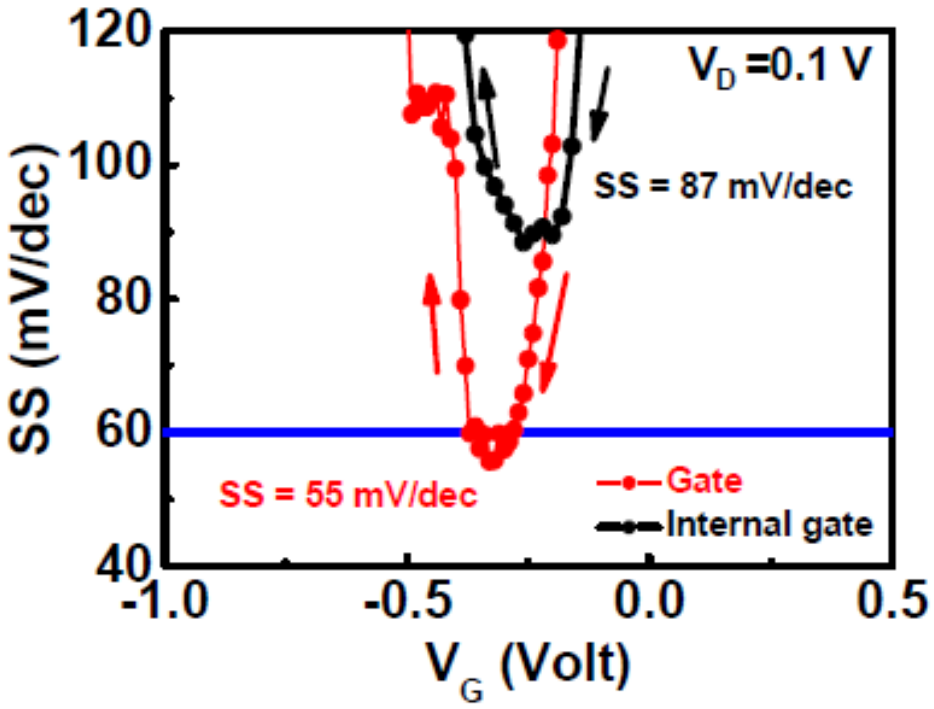
Transconductance (g_m) vs. V_{GS}. The peak g_m is enhanced 118% by the NC integration.

M.H. Lee, IEDM'2013

Hybrid device: Fe FinFET

(*K.-S. Li - IEDM'15*)

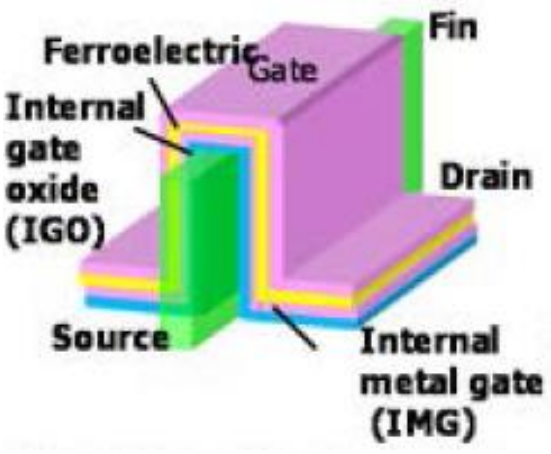


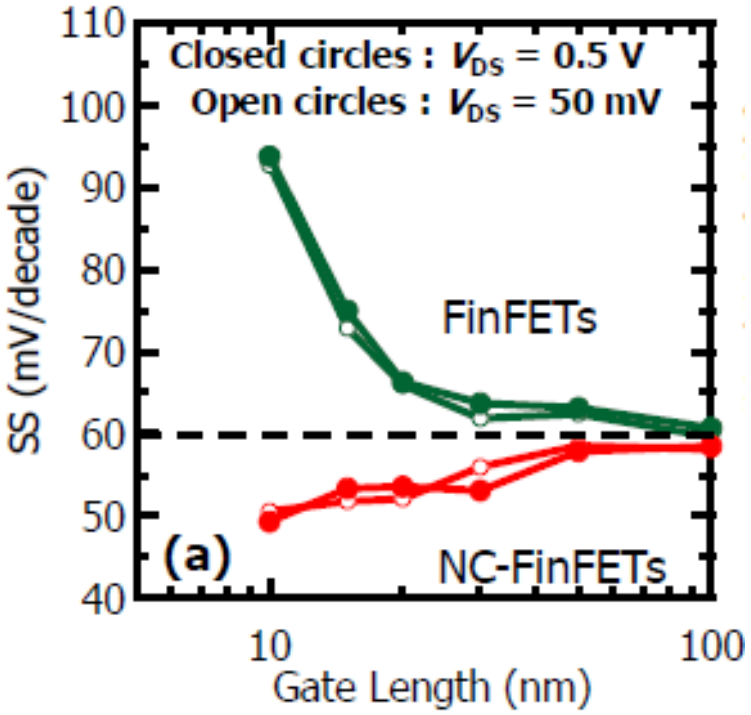


SS ↓ for Fe FinFET / FinFET

Fe material : $Hf_{0.42}Zr_{0.58}O2$

Hybrid device: 3D simulation of NC FinFET / FinFET

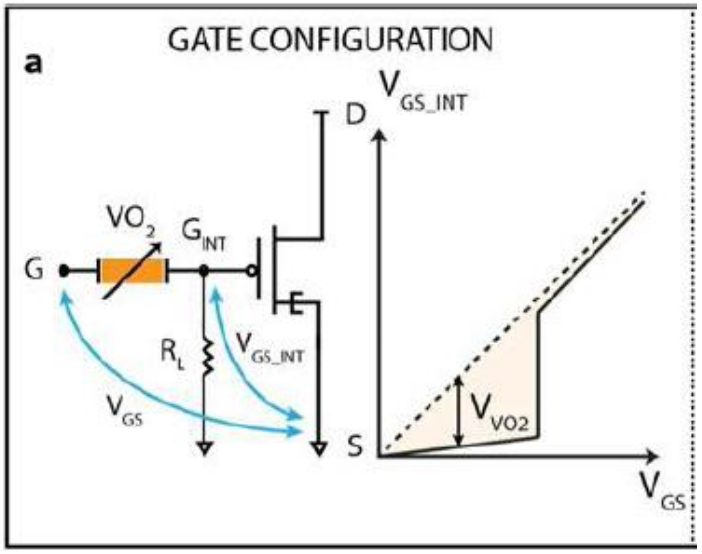


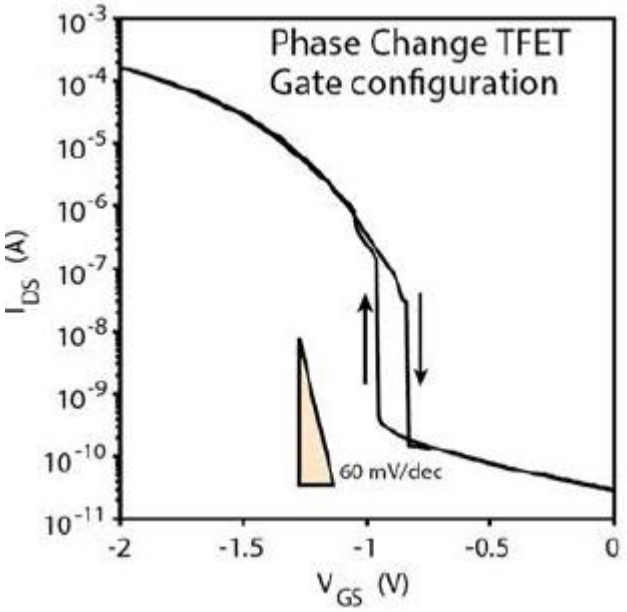


S ↓when Lg ↓ for NC-FinFET with Internal Metal Gate due to reduced DIBL

H. Ota, IEDM 16

Hybrid device: Phase-Change Tunnel FET



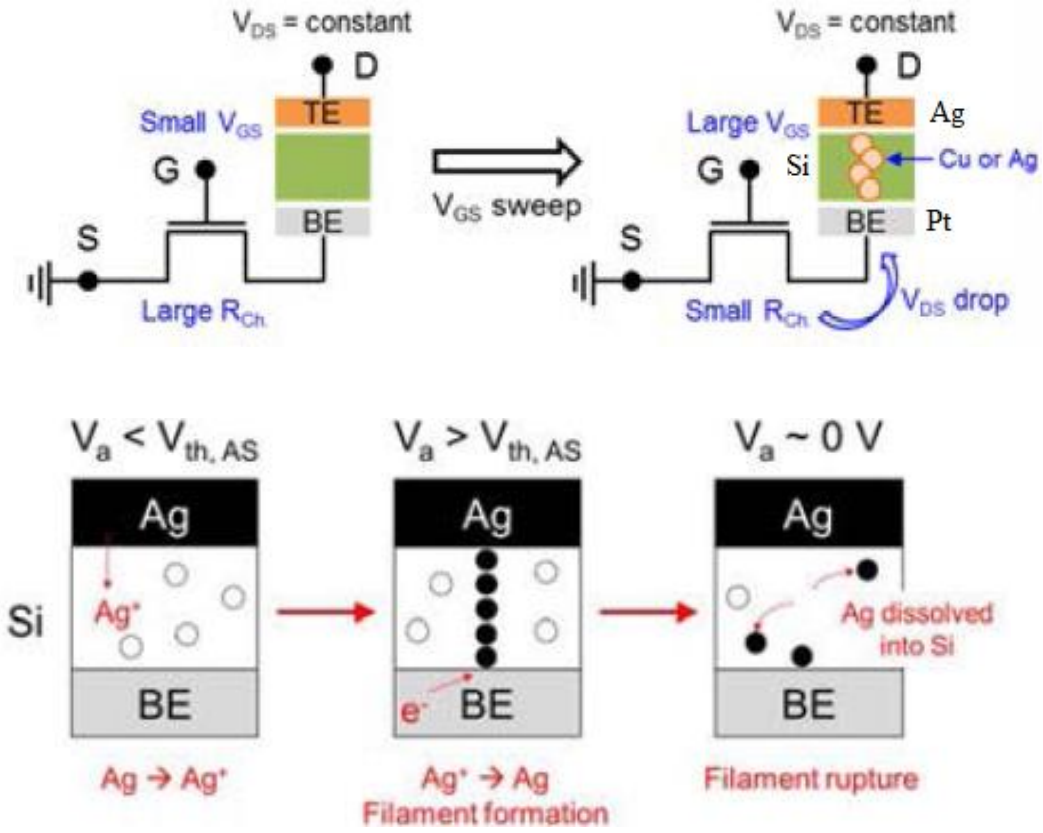


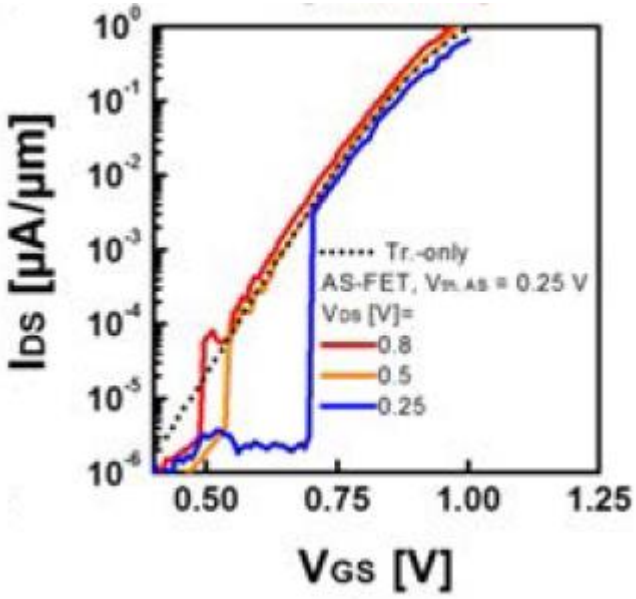
S~4mV/dec for the PC-TFET at 300K for 3 decades of Id

with vanadium dioxide exhibiting a metal-insulator transition by electrical excitation

E.A. Casu, IEDM 16

Hybrid device: Atom-Scale metal filament MOSFET





-Metal filament (Ag, Cu) formed in Si at the Drain with a sufficient V ; breakdown of the filament when V↓

-S~5mV/dec for AS-TFET at Vd=0.25V and 300K for several decades of Id

S. Lim, IEDM 16

Conclusion

- We are facing many challenges, scaling, performance and power reduction which is one of the most important challenge for future nanoscale devices
  =>requires **new physics and device structures** using **many novel materials**
  =>will enable to continue scaling and performance/power improvement

- **FD SOI**, **MG** Devices
- **F.Inv. MG Nanowires or UTB-2D** (with Si, sSi, alternative channel / Ge, III-V, 2D/TMD, BP, HTJ…):

  => *Best SCE, S, Ioff, Vdd, P, Emin for MOS-based architectures* => *Low power/high speed*

- **TFETs** (MG, SOI, GOI, III-V, NW, Strain, HTJ, Grad, QW, 2D), **Hybrid FETs**:

  => **Best Small Slope Switch** up to now
  => BTBT, Fe, PC and AS materials or combination allows for **sub-60mV/dec S** (simulation + experimental results)

  => **TFETs** simulations show promise for very good S, substantial Vdd reduction and high Ion but technology boosters especially **using new materials and devices** and ***additional process improvements are needed to improve real device performance***
  => Applications: *very low power/low-medium speed, Analog/RF, Sensors…*

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Thank you for your attention!

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Sinano Institute Members

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